D4.9 CHIP-LEVEL CHARACTERIZATION FOR PROVIDING PERFORMANCE DATA TO WP5

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EXECUTIVE SUMMARY

PASSION introduces new photonic technologies and devices for supporting agile metro networks, capable of enabling target capacities of Tb/s per channel, 100 Tb/s per link and Pb/s per node over increased transport distances in the range of few hundreds of kilometers. The modularity and programmability (via Software Defined Networks - SDN) of the system components of the node is used to achieve the flexibility and agility level demanded by the dynamic traffic, channel bandwidth/path/state/energy requirements of the metro network.

The PASSION switching nodes function is that of a reconfigurable add and drop multiplexer (ROADM) within the metro core and access networks. The implementation of photonic switches i.e. wavelength selective switches (WSS) and Multicast switches (MCS) in a photonic integrated circuit (PIC) for a node featuring functional aggregation/disaggregation network functionalities are key features of the switching nodes.

This deliverable document reports performance data of on-chip switches developed in PASSION project obtained via experimental characterization. Two implementation approaches are followed in developing PIC switches.The first approach is a monolithic integration, where the passives and the SOA actives are all integrated in the same InP chip. In the second approach, i.e. hybrid integration, the switching functionalities are realized in two target platforms in order to achieve the desired performance, i.e. the passive components are implemented in VTT's SiPh technology while the SOA switching gates are implemented in InP technology.

These realized on-chip switches have been characterized both in a monolithic InP and hybrid SiPh/InP platforms. On monolithic InP both WSS and MCS functionalites has been experimentally demonstrated. A 2x4 MCS with a loss-less performance has been realized. In addition a compact 1x2 WSS, that enables the reduction in footprint in which demultiplexing/multiplexing is enabled by a single arrayed waveguide grating (AWG) is realized. For the hybrid integration of WSS, SiPh passive chip containing AWG deMux/Mux elements and a separate SOA array chip on InP is developed. Flip chip bonding technique developed by VTT is used to realize a hybrid SiPh/InP 10-channel wavelength blocker switch (WBL). Characterization results show promising performance and validate the potential in developing a high port and wavelength count hybrid photonic switch. The first trial assembly SiPh/InP hybrid coupling losses can be improved via the use of on-chip spot-size converters which will relax the tight alignment tolerance. Successful transmission of 10 Gbps and 20 Gbps NRZ data is used to validate the performance of hybrid WBL switch.

Scalability of the switches for supporting high capacity metro network is ensured via a modular approach in which new modules are added to support capacity increase in a pay-as-you-grow manner. This is possible on hybridly integrated SiPh/InP switches thanks to dense density of integration of passives on SiPh and the hybrid flip chip assembly process.

1 INTRODUCTION

1.1 BACKGROUND AND MOTIVATION

The PASSION project works towards the development of application driven photonic technologies supporting innovative transceivers and optical nodes featuring different levels of aggregation (in spectrum, and space) for an envisaged network architecture (shown in Figure 1) which is able to match the growing traffic demand in the metro connections. The PASSION approach is capable of establishing high capacity connection for metro network distances (typically few hundreds of km) with high throughput, low-cost, energy-efficient and reduced footprint devices for massive deployment. End-to-end connectivity for novel services and businesses is achieved with dynamic) SDN control of the different systems and subsystems to ensure metro connectivity and deployment of services. With the introduction of new modular photonic technology devices, PASSION is capable to reach capacity of Tb/s per channel, 100 Tb/s per link and Pb/s per node.

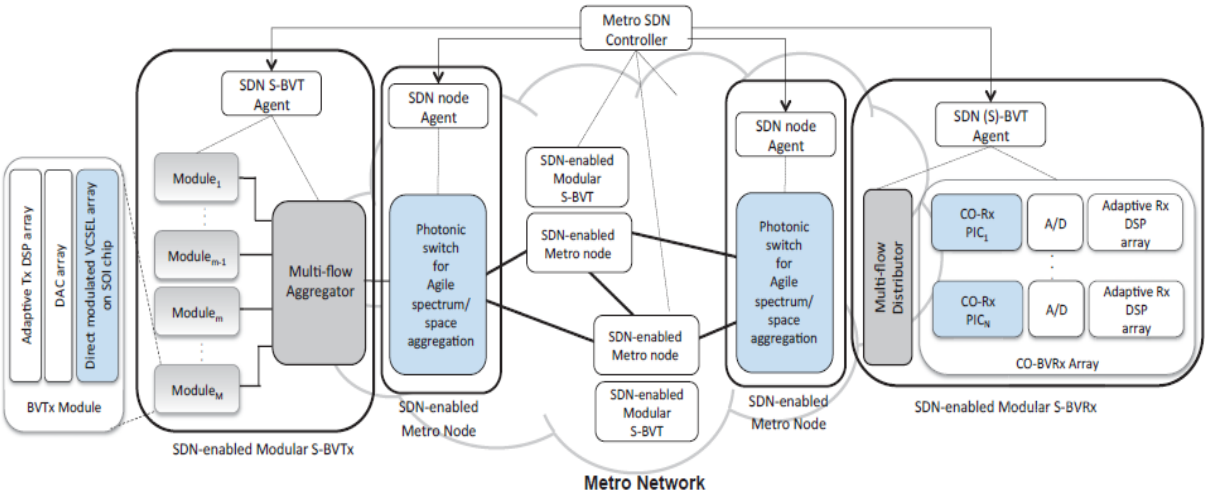


Figure 1 PASSION metro network: envisioned infrastructure, supported by new device technology developments

The growth of internet traffic and particularly bandwidth intensive application such as video, coupled with dynamic and mobile data sources are the driving wheels behind the demand for provisioning of transparent and agile metro networks [1-6]. To effectively utilize the available spectrum and to allow compatibility with the pre-existing transmission systems, it is very essential to develop a node that can efficiently handle dynamic and growing traffic conditions. Furthermore, it is essential that the nodes are equipped with energy-efficient and small-footprint switching technologies given the increasing energy demands of the global telecommunication infrastructure. Current state of the art metro networks are quite static and present limited flexibility and scalability. The metro network architecture within PASSION project will be a key enabler of network flexibility and agility required to address cost and efficiency requirements. Increased system flexibility is adopted with sliceable bandwidth/bitrate variable transmitters (S-BVTs) combined with a node featuring traffic aggregation/disaggregation together with switching in space and wavelength. Increase in the capacity is handled with agile aggregation in the spectrum, polarization and space dimensions while leveraging modularity for scalablity of the nodes.

This metro network concept exploits the SDN paradigm in order to efficiently allocate/use the overall network resources transforming the operation of today's network infrastructure and reducing overprovisioning and margins.

1.2 TARGET OBJECTIVES

The target objective of this deliverable is to report performance data of realized on-chip photonic switches obtained via experimental characterization. The switching functionalities support the flow of traffic within the metro switching node represented in Figure 2. At the metro node, the WDM switching is enabled by wavelength selective switches (WSS) which are implemented in a modular fashion to meet the traffic requirements in which new modules (represented in grey boxes) are added in a pay-as-you-grow scheme. WDM switching enables merging and aggregating/disaggregating tasks on the traffic to maximize resource utilzations by bundling traffic of same destination in a single multi-core fiber (MCF), which is forwarded as bypass traffic in express paths before reaching the destination node in the metro network. Multi-cast switches (MCS) enable contention-less drop signals to the users in conjunction with coherent receiver modules (CRM). In PASSION, we propose the exploitation of semiconductor optical amplifier (SOA)-based gate switches monolithically integrated with passive circuitry on InP and/or hybridly integrated with SiPh circuits to function within the presented novel metro network architecture. In addition to the gating functionalities, booster SOAs are used to provide gain for compensating on-chip losses and achieving low-loss performance.

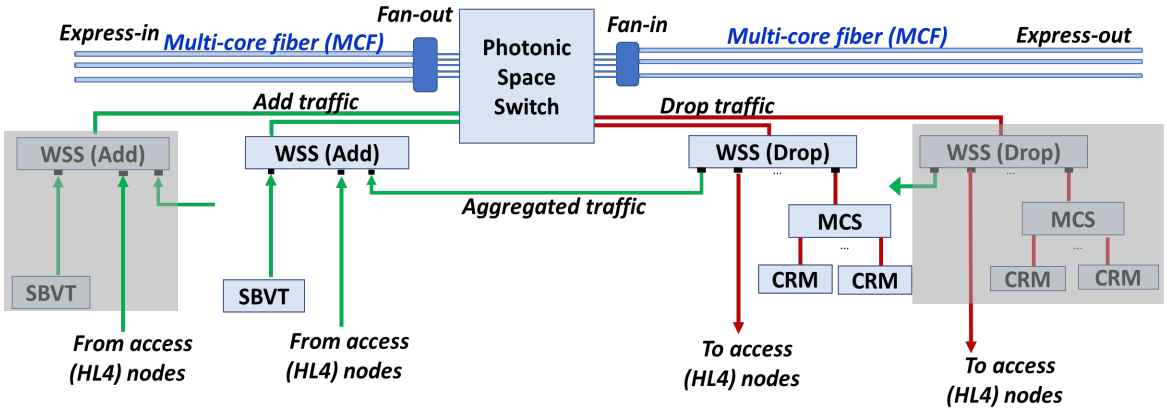


Figure 2 PASSION metro core network: Photonic Space Switch, Wavelength Selective Switch (WSS),Coherent receiver module (CRM)

In this deliverable report, the experimental characterization on the performance of on-chip switches realized both on monolithic InP and hybrid SiPh/InP switches is presented. Specifically, wavelength selective switches (WSS) and multi-cast switching (MCS) developed in monolithic InP platform and hybrid SiPh/InP platform are experimentally characterized.

The measured results will be used to understand current performance and improve subsequent design for possible performance optimization. Design of the switches is presented so as to clearly understand the measurement results. Performance metrics such as insertion loss, extinction ratio, optical signal to noise ratio as well as bit error rate (BER) for a given data transmission capacity will be used for evaluating the performance of the realized photonic switch PICs.

Accordingly, the following set of measurements are presented.

- Experimental characterization of a monlithically integrated InP wavelength selective switch and multicast switch.
- Experimental characterization of a hybridly integrated SiPh/InP wavelength blocker switch

2 MONOLITHIC INP MULTICAST SWITCHES

Combined with CRM, MCS provides cost-effective solution to realize a colorless, directionless and contentionless (CDC) drop within PASSION switching node (given in Figure 2). To achieve a CDC performance, the WSS (Drop) is supported by a multicast switch (MCS) solution for the drop wavelength channels. A MCS splits the drop signals and delivers a copy of all the drop channels to each attached receiver within the CRM. The embedded function of a tunable wavelength filter in the modular WSS employed with the MCS isolates a single drop channel from the selected direction and thus implements contentionless operation at WSS output. The direction-less performance reachablity of a wavelength from any input to any output port is fullfilled. The contentionless attribute is also enabled by the MCS in which the signals at the input ports are broadcast to all output ports irrespective of the wavelength, and the use of space switches at each MCS output port is used to select only one of the input signal and hence generates contention free performance at MCS output.

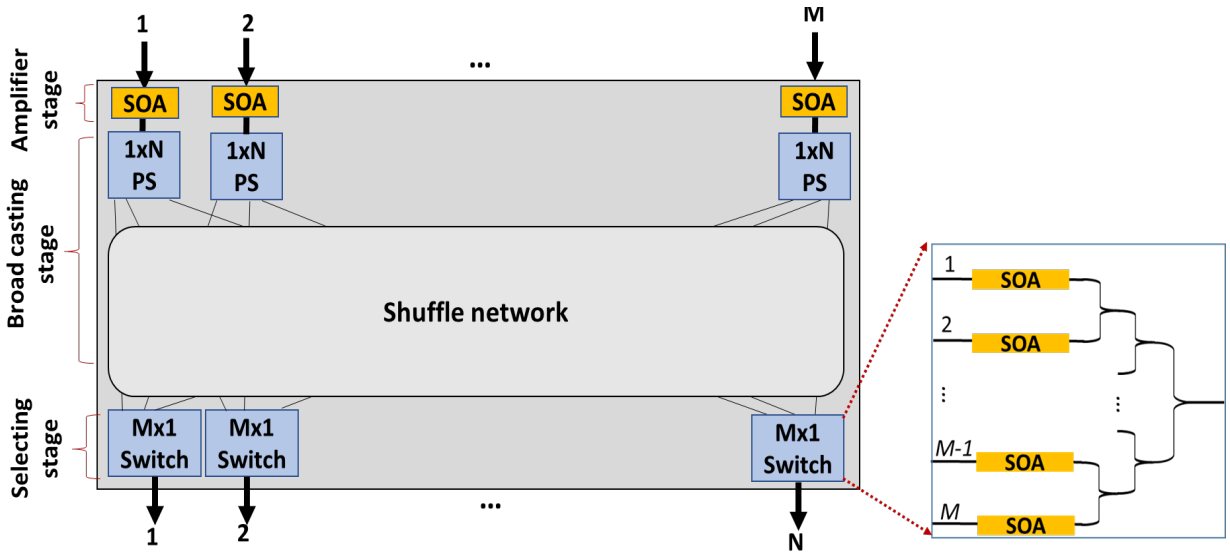


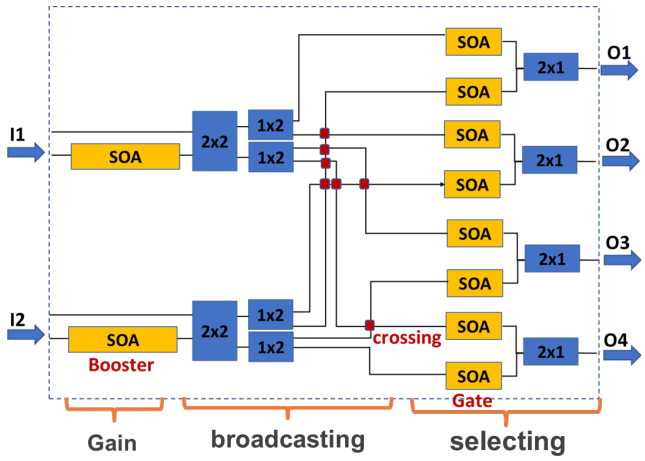
Figure 3 Schematic representation of NxM MCS

Figure 3 shows a typical architecture of a MCS, with *M* input ports and *N* output ports while SOAs are used as switching gates. With its *broadcast-and-select* scheme, the MCS will be able to transfer as many as *N* wavelengths to the attached *N* CRMs. At each of the inputs of the MCS, a *1xN* splitter broadcasts the input signal. For this, an *NM x NM* shuffle network is used to distribute the copies of all input signals from *M* directions to all output ports. The shuffle network is a distribution network made of waveguide crossings.

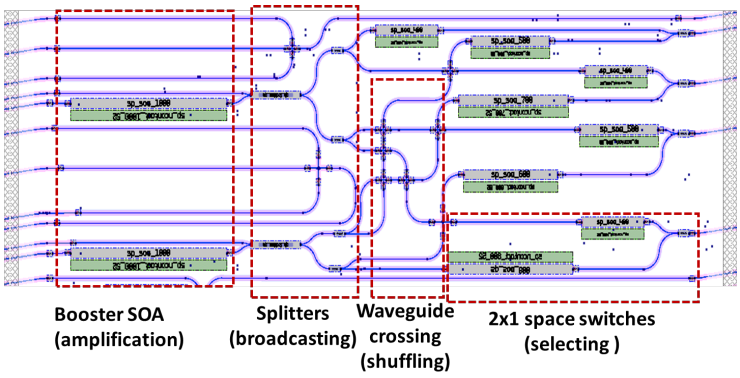
At each of the output ports a *M*x1 space switch is used to select one of the input signals. The Mx1 space switches are based on SOA switching gates and Mx1 power combiners.

On chip power splitting induces an insertion loss 10log(*N*) dBs. On the other hand, the power combiner within the Mx1 switch at the output port brings insertion loss of 10log(*M*) dBs. Inorder to compensate the on-chip losses, a booster SOA is used at each of the input ports. The booster SOA placed at the input ports is used to maintain a high OSNR at the output ports.

To demonstrate the MCS functionality, a 2x4 monolithically integrated MCS module is designed and fabricated at SMART photonics foundry. In the next section, the design and experimental characterization of the 2x4 MCS is presented.



(a)



(b)

Figure 4 (a) Schematic representation of 2x4 MCS (b) mask layout of a 2x4 monolithic MCS on InP

2.1 Design of 2x4 MCS

Figure 4(a) shows the schematic representation of a monolithically integrated 2x4 MCS on InP, and Figure 4(b) shows its mask layout. The amplification stage is implemented by booster SOAs that are used to compensate the loss of splitters in the broadcasting stage. The broadcasting stage is implemented using 2x4 MMI power splitter which incurres an insertion loss of 6 dBs. The broadcasted signals are then distributed via waveguide crossings. At each of the 4 output ports of the MCS, 2x1 space switches are used to select the desired signal. The 2x1 space switches are made of SOA gates connected with a 2x1 MMIs. Within the 2x4 MCS, the signal passes through a

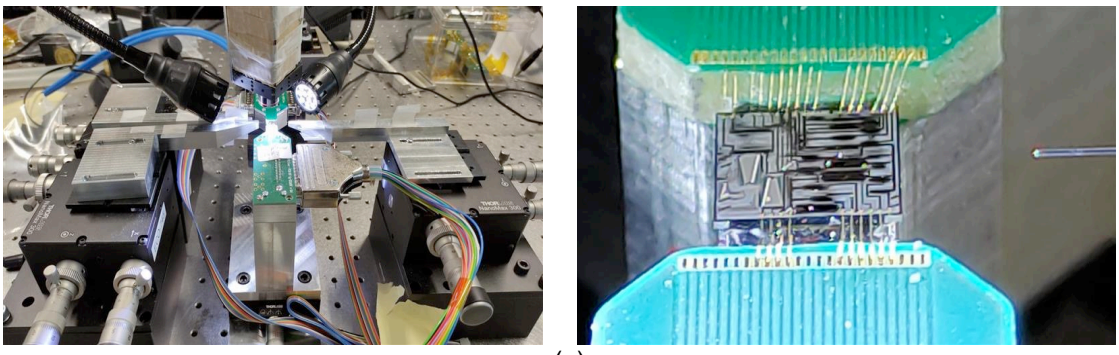
Table 1 Design specification of booster and gate SOAs with in MCS

SOA	Length (µm)	SOA	Length (µm)
Booster1	1000	Gate 4	700
Booster2	1000	Gate 5	500
Gate 1	400	Gate 6	600
Gate 2	500	Gate 7	400
Gate 3	400	Gate 8	800

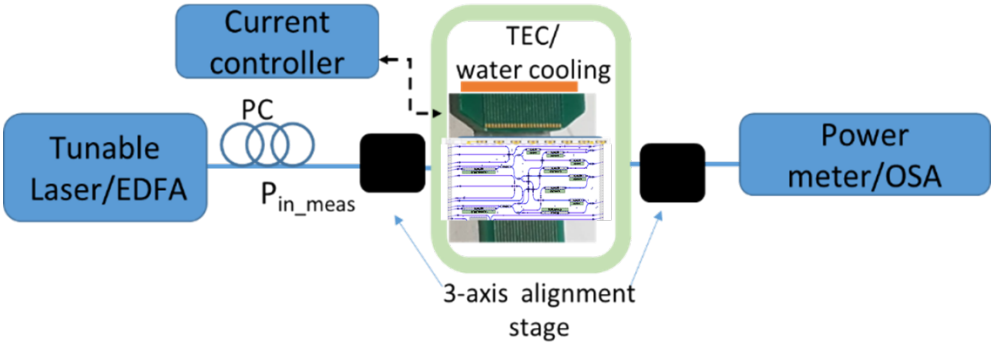
maximum of 4 waveguide crossings which have a total insertion loss of 1 dB or less.The 2x1 MMIs bring additional loss of 3 dBs, bringing the total onchip loss in the range of 9 -10 dBs.Therefore, the booster SOAs are 1000μms long to provide enough gain for compensating on-chip losses. Table.1 lists the length (μm) of the two booster SOAs and 8 gate SOAs.

2.2 CHARACTERIZATION RESULTS

The photograph of the realized monolithic InP is in Figure 5(a). The PIC is wirebonded on a PCB board for easier access of the electrical contacts.Then, the PIC is mounted on fiber-to-chip coupling setup where 3-axis stages are used to couple light in and out of the PIC. The schematic characterization setup is shown in Figure 5(b). A current controller is used to supply power supply to the SOAs. The electrical and optical characterstics of 2x4 MCS circuitry is presented.



(a)



(b)

Figure 5 (a) photograph of the realized photonic chip and fiber-chip coupling setup (b) Schematic of fiber-to-chip coupling setup, tunable source/ EDFA noise source / power meter and Optical spectrum analyzer

2.2.1 Electrical characterization: SOA I-V curve

A 2x4 MCS consists of ten SOAs, two booster SOAs and 8 gate SOAs. The current vs voltage (I-V) curve of these SOAs is measured and is given in Figure 6. Eight of the ten SOAs exhibit the typical I-V curve of an SOA and therefore are operational.The other two gates SOAs don't exhibit the typcial I-V curve of a diode and are therefore not operational. As a result, two out of eight I/O paths connected by these two SOAs are not operational and therefore no optical power was collected for these paths.

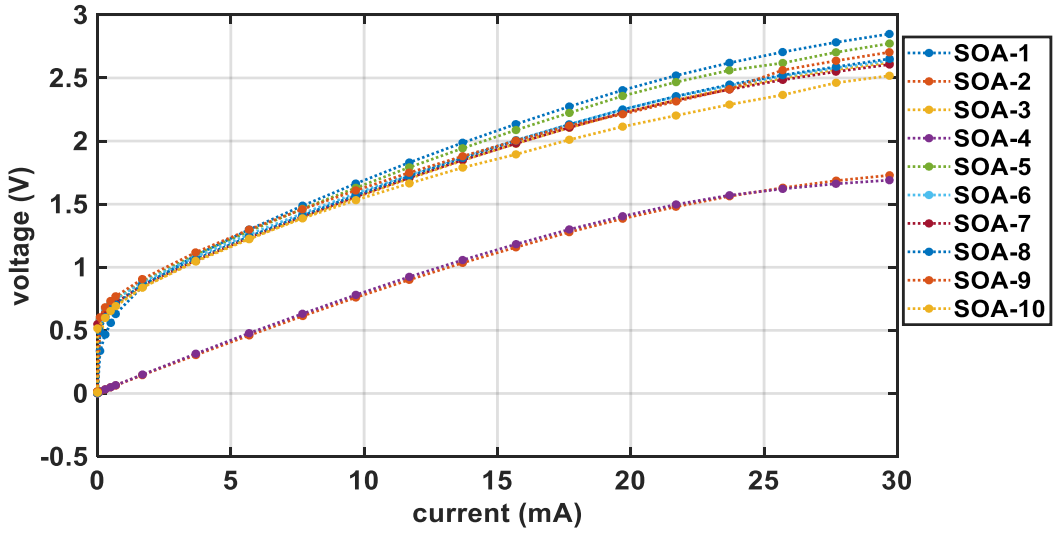


Figure 6 I-V curve of SOAs within MCS

2.2.2 Optical characterization:SOA ASE profiles

Next the SOAs in the MCS structure are optically characterized by measuring the amplified spontaneous emission (ASE) profile by collecting the optical power at the output ports of the MCS (for the gates and at the input ports of the MCS for the booster SOAs). The ASE profile of the SOAs are given in Figure 7 while the booster current is varied between 0 and 120 mA and for 50 mA of current applied on the gate SOAs. Both of the booster SOAs are fully functional and showing signs of saturation after 100 mA of current. Six out of eight gate SOAs are operational. The other two gate SOAs are not functional as expected from their not so good I-V curves. The ASE profiles are measured between 1500 nm to 1600 nm and the gain peak is centered at 1550 nm.

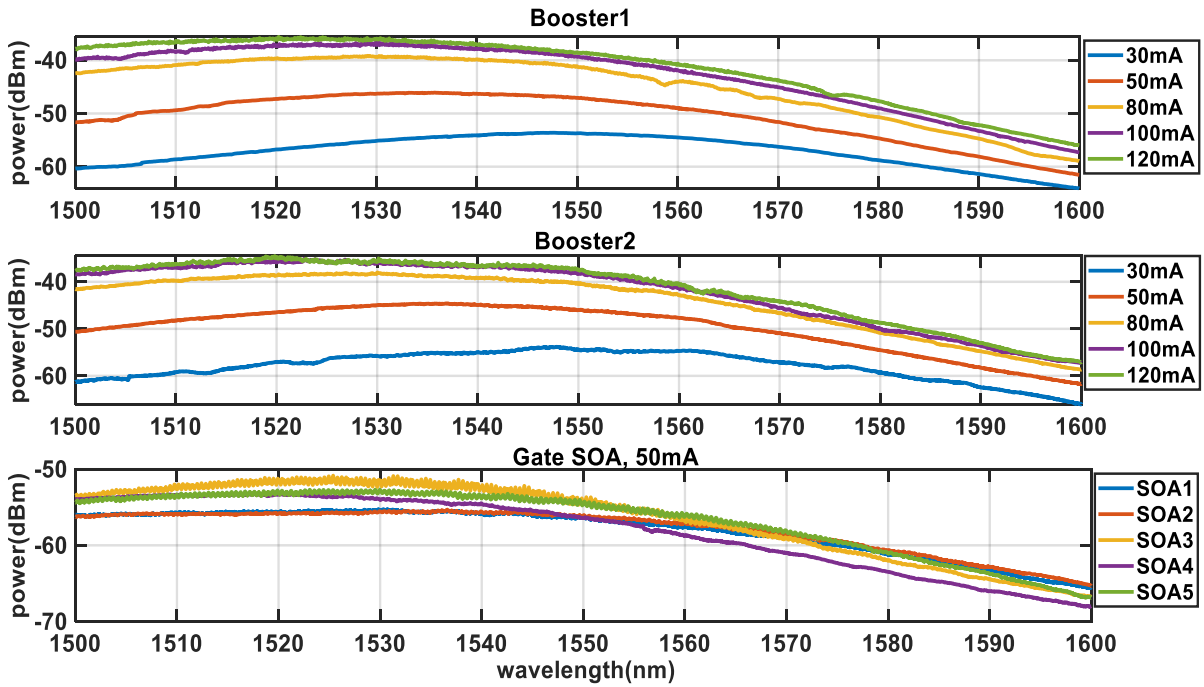


Figure 7 ASE profile of the booster and gate SOAs of the MCS

2.2.3 2x4 MCS fiber to fiber transmissions

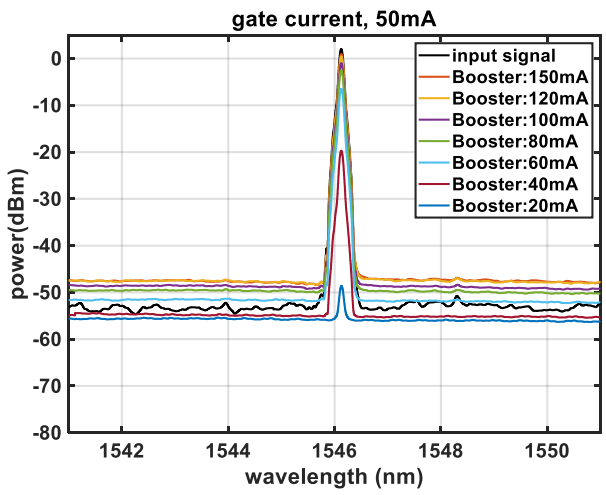
Between the 2 input ports and the 4 output ports of the MCS switch, there are 8 optical paths providing connectivity. 6 paths out of 8 are operational and were characterized in terms of fiber-to-fiber transmission, output OSNR, switching extinction ratio.

Fiber-to-fiber transmission: a laser light with 1546.1 nm emission, corresponding to the SOA gain peak, was injected into the MCS. The fiber-to-fiber transmission is obtained by normalizing the measured output power with respect to the input power. Two input power values, namely -10 dBm and +2dBm are injected into the input lensed fiber to evaluate the dependence of the gain characterstic with respect the input power. During the measurement, the booster current is varied

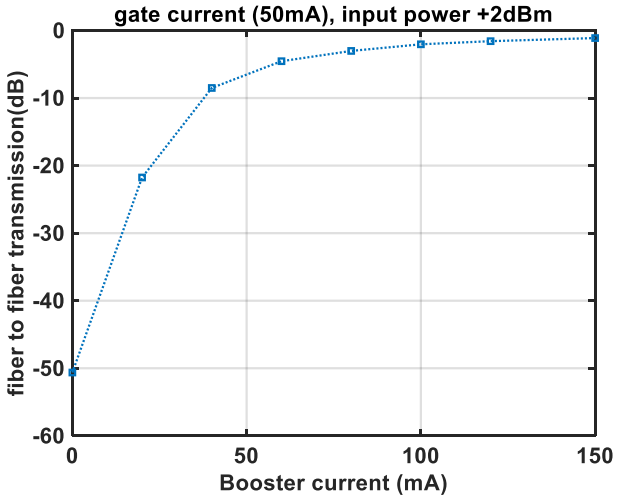
between 0 and 150 mA and the gate current is varied between 0 and 80 mA. These measurements were repeated for all functioning 6 paths.

At first the path I1=> O4 was evaluated, and the obtained results are given in Figure 8 and Figure 9. Figure 8 shows the collected spectrum of the output signal [dBm] and the fiber to fiber transmissions [dB], for different values of the booster and gate current, while an input signal of +2 dBm is used.

First the gate current is fixed at 50 mA, and the booster current is swept between 0 and 150 mA.It can be seen from Figure 8(a) and Figure 8(b), that the fiber-to-fiber transmission of -1 dB is obtained for 150mA of booster current and 50mA of gate current. Furthermore, signs of saturation is observed at 100mA booster current. Next the booster current is fixed at 80mA and the gate current is swept between 0 and 80mA. It can be seen from Figure 8(c) and Figure 8(d) that the fiber-to-fiber transmission of -1.8 dB is achieved for booster current of 80 mA and gate current of 80 mA. Gate SOA can achieve an extinction ratio of 33 dB.



(a)



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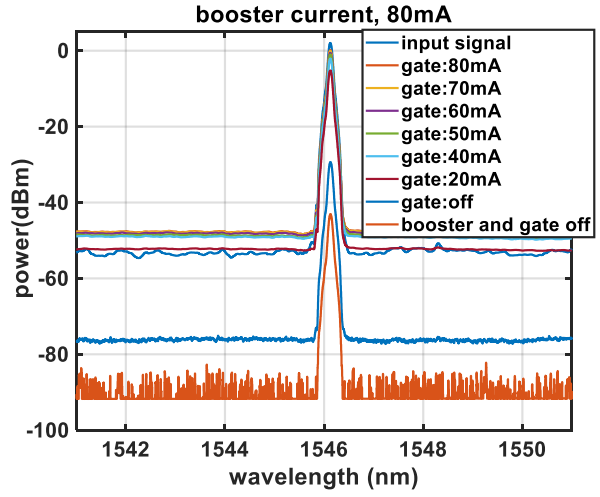
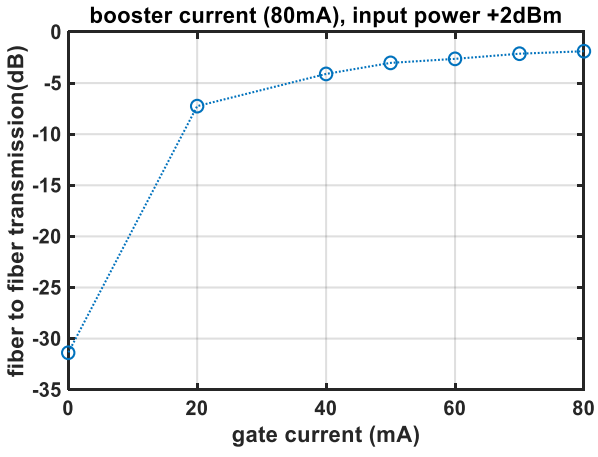


(c)



(d)

Figure 8 Path O1=> O4, input power of +2dBm (a) Output signal of MCS , booster current 0 -150 mA, gate current 50mA (b) fiber-to-fiber transmission (c) Output signal of MCS , booster current 80 mA, gate current 0-80mA (d) fiber-to-fiber transmission

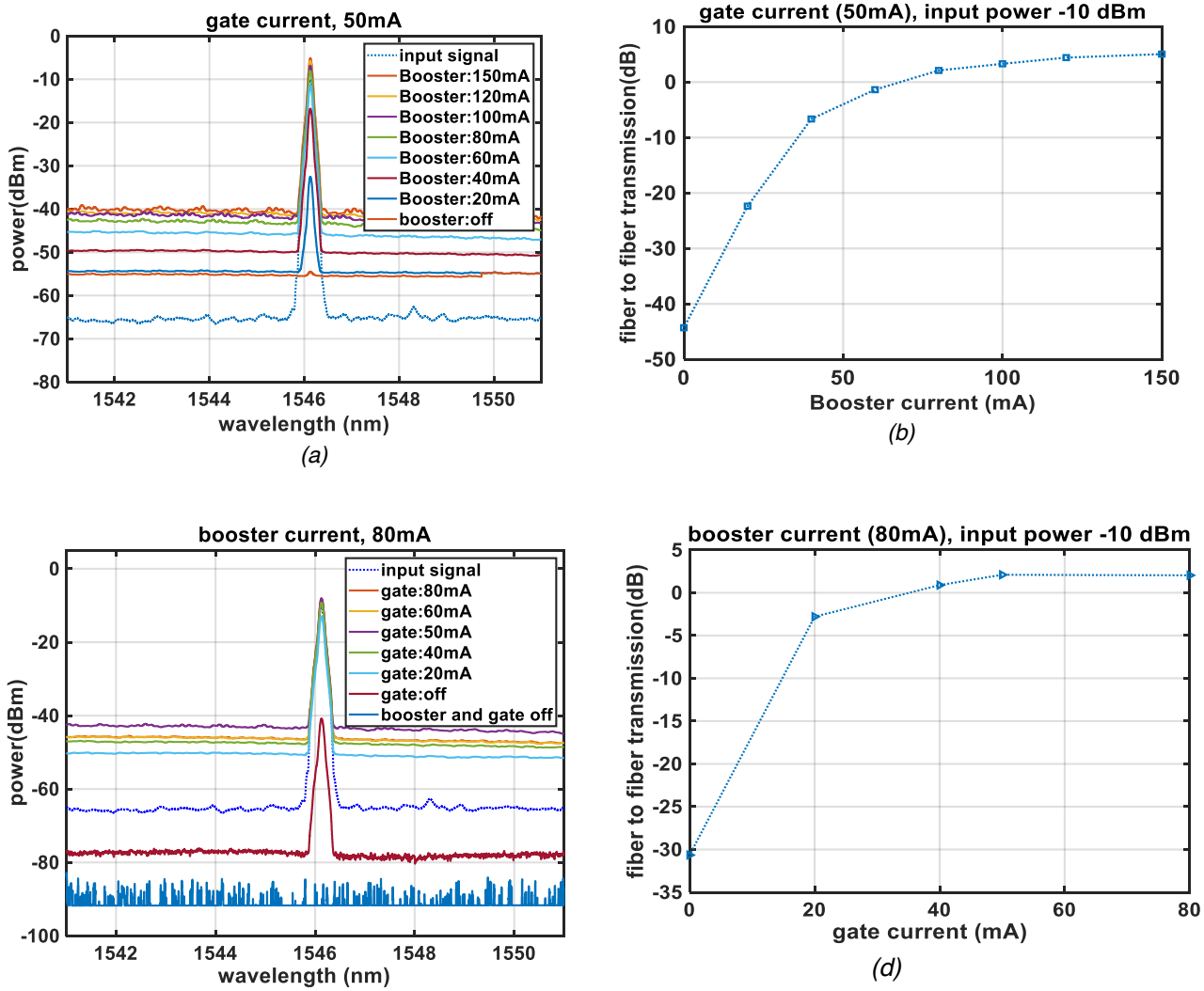


Figure 9 Path O1=> O4, input power of -10 dBm (a) Output signal of MCS , booster current 0 -150 mA, gate current 50mA (b) fiber-to-fiber transmission (c) Output signal of MCS , booster current 80 mA, gate current 0-80mA (d) fiber-to-fiber transmission

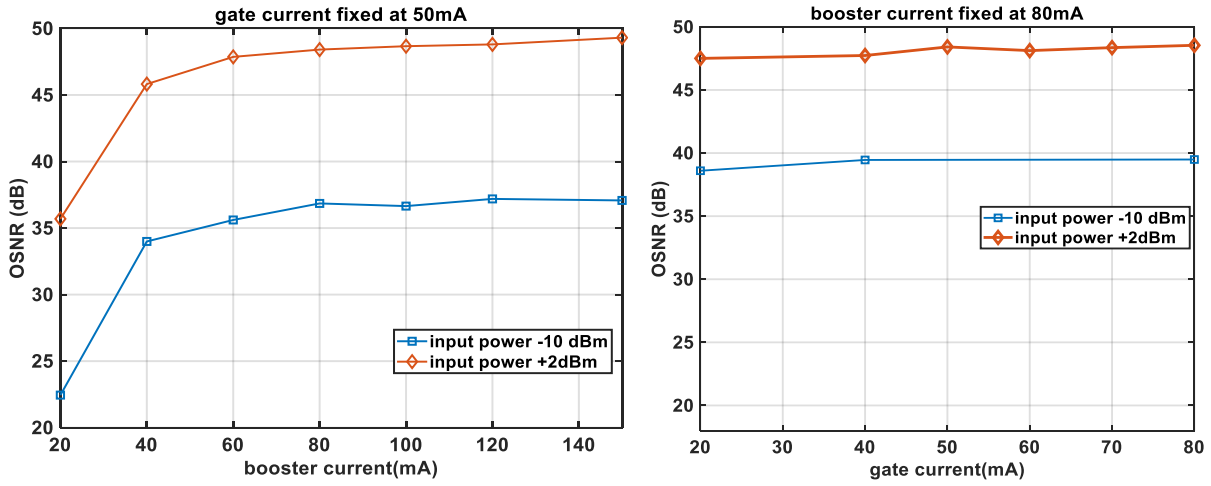
Next the path I1 => O4 was tested, by injecting 50 mA of current on the gate SOA and by sweeping the booster SOA from 0 mA to 150 mA, the input power is fixed at -10dBm. The ouput power measured in each case is given in Figure 9(a). The MCS enables a fibre-to-fibre gain of 5 dB as shown in Figure 9(b) when booster current is tuned at 150 mA. These corresponds to total gain of 26 dB, since the on-chip loss of 9 dBs by the 2x4 MMI splitter and 2x1 MMI combiners and 2x6 dB of fiber to chip coupling losses. It can be noticed that the booster starts to show signs of saturation after 100 mA. Next the booster current is fixed at 80mA and the gate current is varied between 0 and 80 mA and the collected power is given in Figure 9(c). A fibre-to-fibre gain of 3 dB as shown in Figure 9(d) is achieved when 80 mA is applied on both gate and booster SOAs, corresponding to a combined gain of 24 dB. Furthermore, the booster current is the most important one since it is possible to lower the gate current to 20 mA, corresponding to transparency, without significantly impacting the overall gain. This is an important aspect for the energy efficiency of MCS. By varying the gate current between 0 and 80 mA, the extinction ratio of 33 dB is achieved.

Output OSNR :

The OSNR of the output signal for path I1=>O4 is monitored under two input power values of -10 dBm and +2 dBm injected into the input fiber. Different values of booster current varying between 20 and 150 mA and gate current varied between 20 mA and 80mA are employed and the measured OSNR [dB] vs current [mA] are shown in Figure 10(a) and Figure 10(b) respectively.

First the gate current is fixed at 50 mA and the booster current is varied between 20 mA and 150 mA. It can be seen from Figure 10(a) that for +2 dBm of input power, 49 dB of OSNR is obtained for a booster current of 150 mA and 50 mA of gate current. For the same current values and -10 dBm input power, a lower OSNR value of 36 dB is measured.

Next the booster current is fixed at 80 mA and the gate current is varied between 20 mA and 80 mA. The OSNR is between 45 dB – 48 dB when the input power of +2dBm is used and between 38 dB - 39 dB for -10 dBm of input power. Furthermore, it can be seen that the OSNR is independent of the gate current, this is because the booster SOA is the first gain element in the MCS path providing the OSNR boost. This an important aspect of the MCS functionality, in enabling energy efficiency, since the gate current can be operated in low current value of 20mA (at transparency point), without affecting the output OSNR.



(a) *(b)*

Figure 10 Output OSNR (a) gate current fixed at 50mA (b) booster current fixed at 50mA

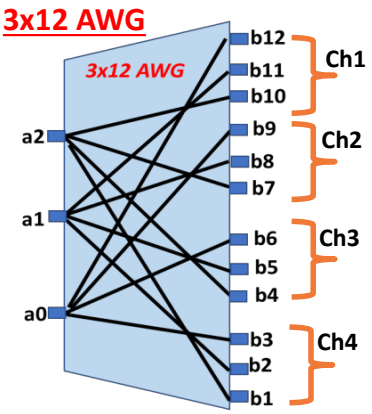
All other paths :

These experimental characterizations were repeated for the remaining paths of the MCS. Out of the 8 possible paths, the 5 operational paths showed the expected performance, as summarized in Table 2.

The fibre-to-fibre transmission ranges from a gain of +2 dB to -3.4 dB when -10 dBm input power is used. The output OSNR is also monitored for two input power levels at -10 dBm and +2 dBm. The output OSNR ranged between 35 – 39 dB in case of -10 dBm input power, and 45-47 dB in case of +2 dBm input power. The number of waveguide crossings did not pose performance limitation, indicating the potential for successful realization of higher port count MCSes. These experimental results show promising prospects toward high port count and high connectivity MCSes by the following modularity feature characterizng the PASSION design.

Table 2 Input/output connectivity and transmission performance of 2x4 MCS

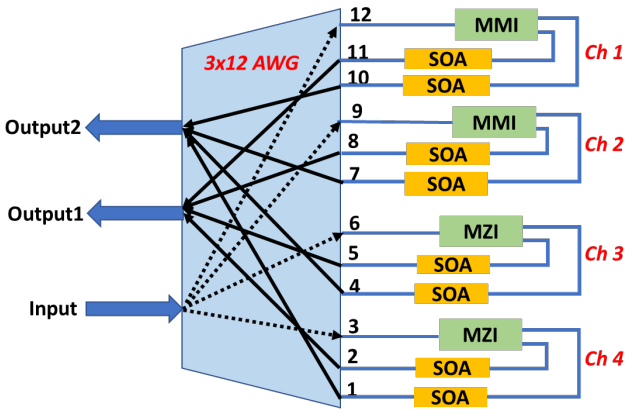
Path	I/O mapping	Gate (μm)	Number of crossings	Fiber to fiber (dB) transmission @ -10 dBm input power	Output OSNR (dB)	
					Input power of -10 dBm	Input power of +2dBm
1	I1-> O4	400	3	+2	39	47
2	I1->O3	500	2	0	35	47
3	I1->O2	400	1	Not so good, -38 dB,	-	-
4	I2->O2	700	3	2 dB	37	45
5	I2->O3	600	1	+2 dB	37	47
6	I2->O1	500	4	-3.4dB	36	46



(a)

Ch	wavelength	Port combinations
1	$?_0$	a0,b3 ; a1,b2; a2,b1
2	$?_1=?_0$+400 GHz	a0,b6; a1,b5; a2,b4
3	$?_2=?_0$+800 GHz	a0,b9; a1,b8; a2,b7
4	$?_3=?_0$+1200 GHz	a0,b12; a1,b11; a2,b10

(b)



(c)

Figure 11 (a) Schematic representation of 3x12 AWG (b) input/output port combination (c) schematic representation of a 1x2 WSS in a folded configuration

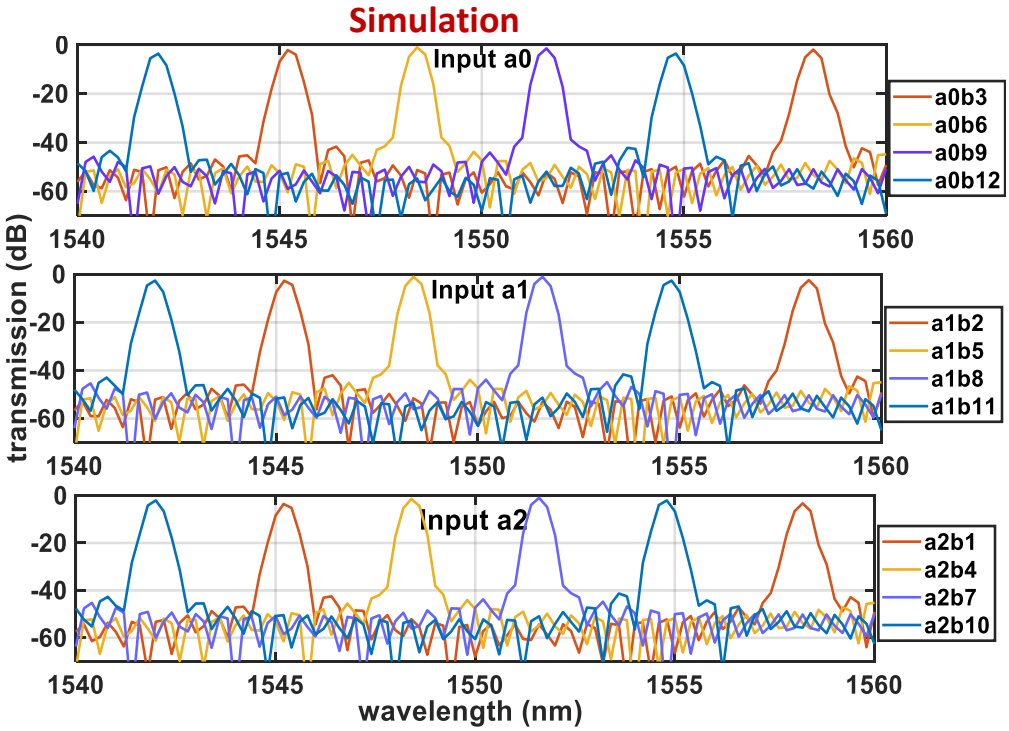


Figure 12 Simulation results of the transmission spectrum of a 3x12 AWG

3 MONOLITHIC INP WAVELENGTH SELECTIVE SWITCHES

The monolithic implementation of the WSS units in InP targets the design of passive deMux/Mux units together with SOA actives in a single InP chip. To demonstrate this capability, a compact 1x2 WSS is designed and realized. This design is based on a single 3x12 AWG and reduces the number of required AWGs by three and leads to a compact design. In this chapter, the design and characterization of the 1x2 WSS is given.

3.1 DESIGN OF 1X2 WSS

For monolithic WSS a compact 1x2 WSS was designed and experimentally characterized. The performance results show promising prospect on all InP monolithic switches. The design is based on a single 3x12 AWG, a 1x2 WSS switching of 4 channels. The schematic representation of the design is given in Figure 11. Figure 11(a) and Figure11(b) show the schematic representation of a 3x12 AWG and the AWG port combinations for each of the four channels. For the given port combinations, the 3 consecutive output ports of the AWG spectrally overlap. The 12 output ports of the AWG then correspond to 4 spectral channels (Ch1,…,Ch4) spaced 400 GHz apart. This enables these ports to be connected to obtain a 1x2 WSS switching. Figure 11(c) shows the schematic representation of a 1x2 WSS in which SOA gate and SOA+MZI gates are used. For instance for a WDM signal entering port a0, it will be demultiplexed to output ports b3, b6,b9 and b12. Then these channels will be split (broadcasted) by a 1x2 MMI to ports (b2,b1); (b5,b4); (b8,b7) and (b11,b10) by turning on the respective switching gates. At these ports ((b2,b1); (b5,b4); (b8,b7) and (b11,b10)) the signals will be multiplexed to output1 and output 2. The switching gates therefore enable blocking or passing of the signal toward the output ports. Ch1 and Ch2 have an SOA switching gate which is 500 μm long, while Ch3 and Ch4 have a switching gate based on a 300 μm long SOA connected with MZI switch. Since the extinction ratio of MZI switches aids the extinction ratio of the gate SOAs, the SOAs for Ch3 and Ch4 are 200 μm shorter than the SOA gates of Ch1 and Ch2. Figure 12 shows

the simulated response of the 3x12 AWG for 400 GHz channels. One can notice that channels plotted in the same color has the desired spectral overlap according to the given port combination.

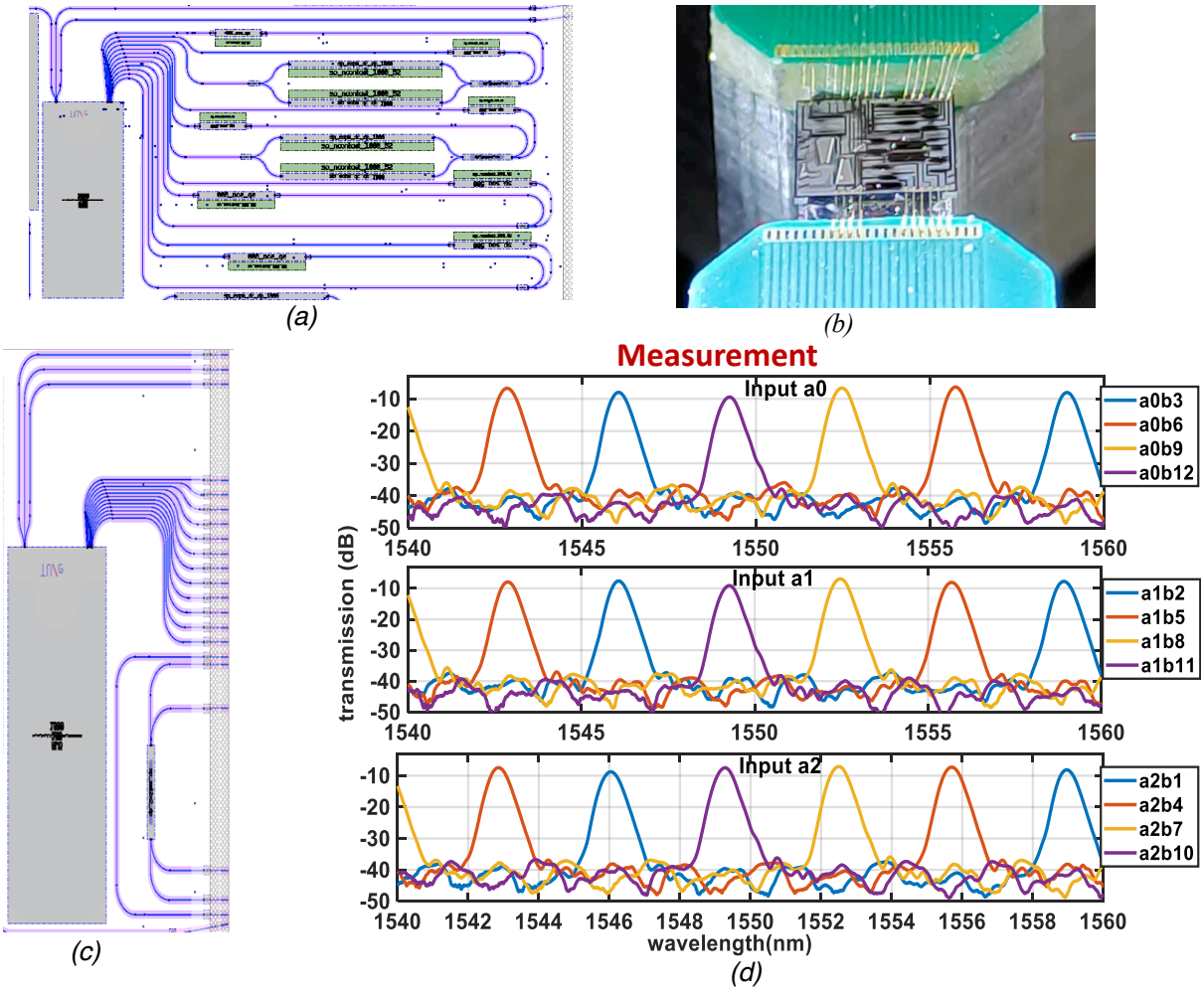


Figure 13 Mask layout of 3x12 AWG (b) photograph of the realized monolithic WSS (c) mask layout of a 3x12 AWG (d)measured transmission characteristic of 3x12 AWG

3.2 Characterization Results

Figure 13(a) shows the mask layout of the 1x2 WSS and Figure 13(b) shows the photo of the realized 1x2 WSS mounted on fiber-coupled measurement set up. In addition to the 1x2 WSS, test structures of 3x12 AWG, SOA switching gates and 1x2 MZIs were characterized.

3.2.1 3x12 AWG

Figure 13 (c) shows the mask layout of 3x12 AWG test structure. Figure 13(d) shows the transmission characteristics of 3x12 AWG, for given port combinations in Figure 12(b). The measured results are similar to the simulated response given in Figure12. The transmission spectrum was obtained by using EDFA wideband ASE as the input and the obtained spectrum in Figure 13(d) is normalized with respect to the input. It can be clearly seen that the combinations represented by the same color plot spectrally overlap, as desired. Furthermore, the channel spacing is the same as the design value of 400 GHz.

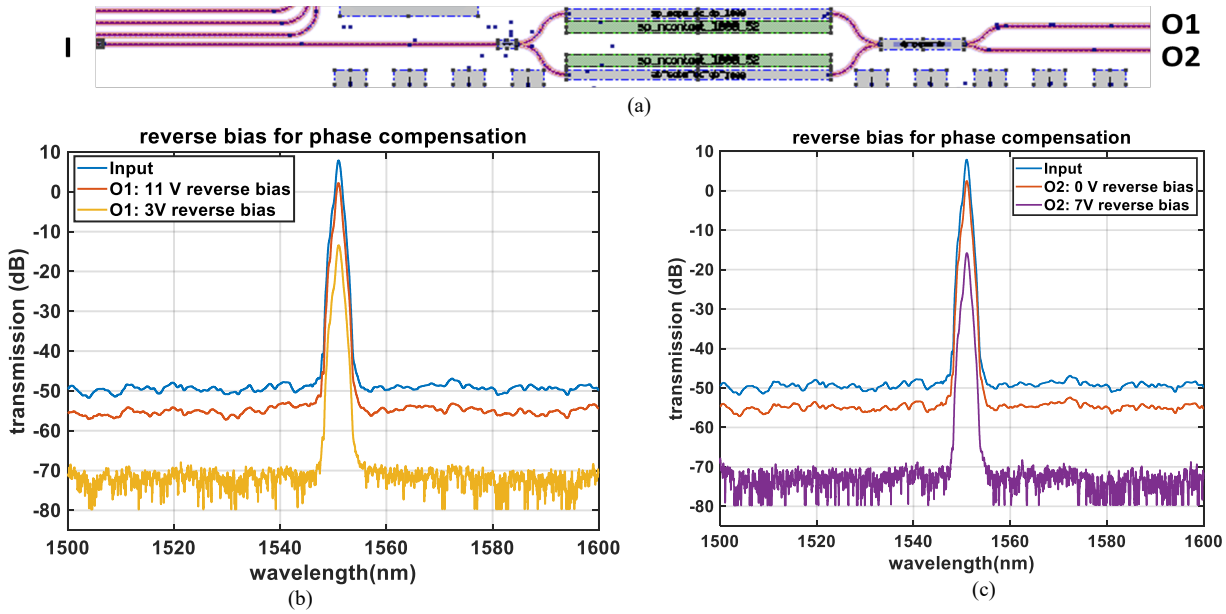


Figure 14 (a) 1x2 MZI switch (b) full or suppressed transmission through the MZI switch, output port O1 (c)) full or suppressed transmission through the MZI switch, output port O2

The insertion loss of each channel is measured by injecting a laser light centered at the central wavelength of the AWG channels. The insertion loss ranges between 3 and 5.8 dB. The signal to crosstalk level is more than 30 dB. The obtained spectral matching between the port combination shows 1x2 switching capability enabled by the 3x12 demultiplexing/multiplexing AWG.

3.2.2 MZI switching gates

The MZI switching gate structure shown in Figure 14(a) was characterized. It is a 1x2 switch where the signal is switched from input port I to output port 1 (O1) or output port2 (O2). Two phase modulators which are 1000μm long are placed on the two arms of the MZI to enable the switching of the signal to the desired output port. These phase modulators are reversely biased in order to induce electro-optic phase shift.

Figure 14(b) and Figure 14(c) show the full transmission spectrum and the suppressed transmission spectrum at the two output ports O1 and O2. When no voltage is applied to the two arms of the MZI most of the power is routed to the output port O2. This corresponds to coupling ratio of 0.025 :0.975 between output ports O1:O2. Next 11V reverse bias is applied to switch the signal to output port O1 for full transmission as can be seen in Figure 11(b). And to fully switch the signal to output port1 reverse bias of 3V is applied. In case of O2, full transmission is achieved with 0V of reverse bias, and switching to the O1 via suppressed transmission is achieved with a reverse bias of 7V.

In both cases full transmission incurrs an insertion loss of 5 dB and the extinction ratio in case of suppressed transmission is 15.5 and 18 dB for output ports O1 and O2 respectively.

3.2.3 1x2 WSS

The realized 1x2 WSS whose mask layout is given in Figure 13(a) is characterized by measuring the ASE profiles of the gate SOAs at the input port and at the two output ports. Two SOAs namely SOA1 and SOA2, corresponding to output ports Output1 and Output2, are turned on to measure the respective ASEs as shown in Figure 15. It can be seen that four plots with the label Input:SOA1, Input:SOA2, Output1:SOA1, Output2:SOA2 spectrally overlap at wavelengths 1549.78 nm, 1553 nm, 1556.2 nm and 1559.4 nm for Ch1, Ch2, Ch3 and Ch4 respectively. These corresponds to the design wavelength of the WSS channels with 3.2 nm (400 GHz) spacing.

One can note from Figure 15 that the spectral overlap between the input and the output ports is maintained by either turning on SOA1 or SOA2. In other words, if one wants to send the input signal to output port 1, SOA 1 needs to be turned *On*, and if its is desired to send the input signal to output port 2, SOA 2 needs to be turned *On*. By turning on both SOA1 and SOA 2 at the same time, the input signal is broadcasted to both output ports. This further verfies the realization of the 1x2 WSS functionaity.

To evaluate the insertion loss and the switching performance of the WSS a laser light is injected into the input port of the WSS, centered at the four wavelength channels (Ch1 at 1549.78 nm, Ch2 at 1553 nm, Ch3 at 1556.2 nm and Ch4 at 1559.4 nm). The signal at the Output port (Output1) of the WSS is measured and is given in Figure 16.

The insertion loss ranges between 7 dB for Ch2 to 12 dB for Ch4. This measurement is line with 2 x 5 dB insertion loss within the AWG (since the signal traverses the AWG twice for demultiplexing and

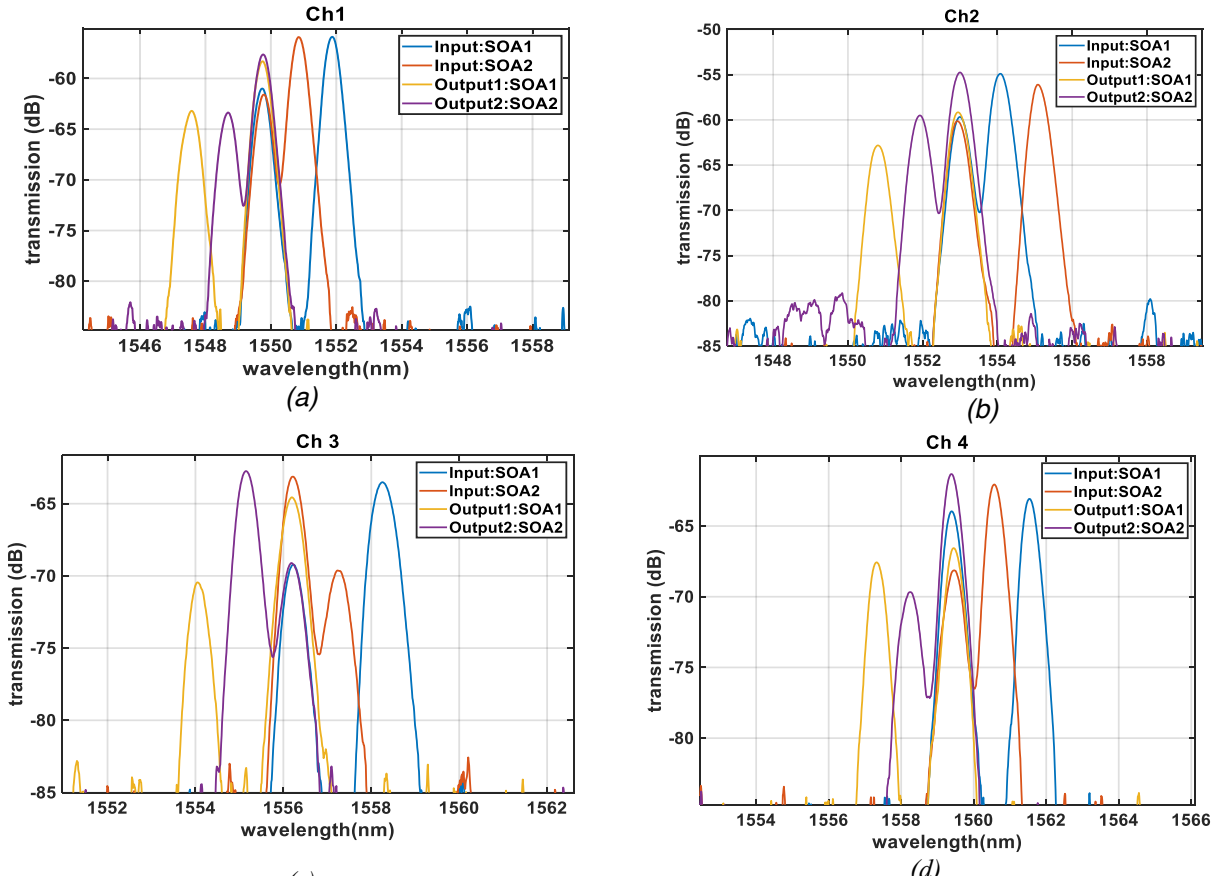


Figure 15 measured ASE spectrum (a)Ch1 (b) Ch2 (c) Ch3 (d) Ch4

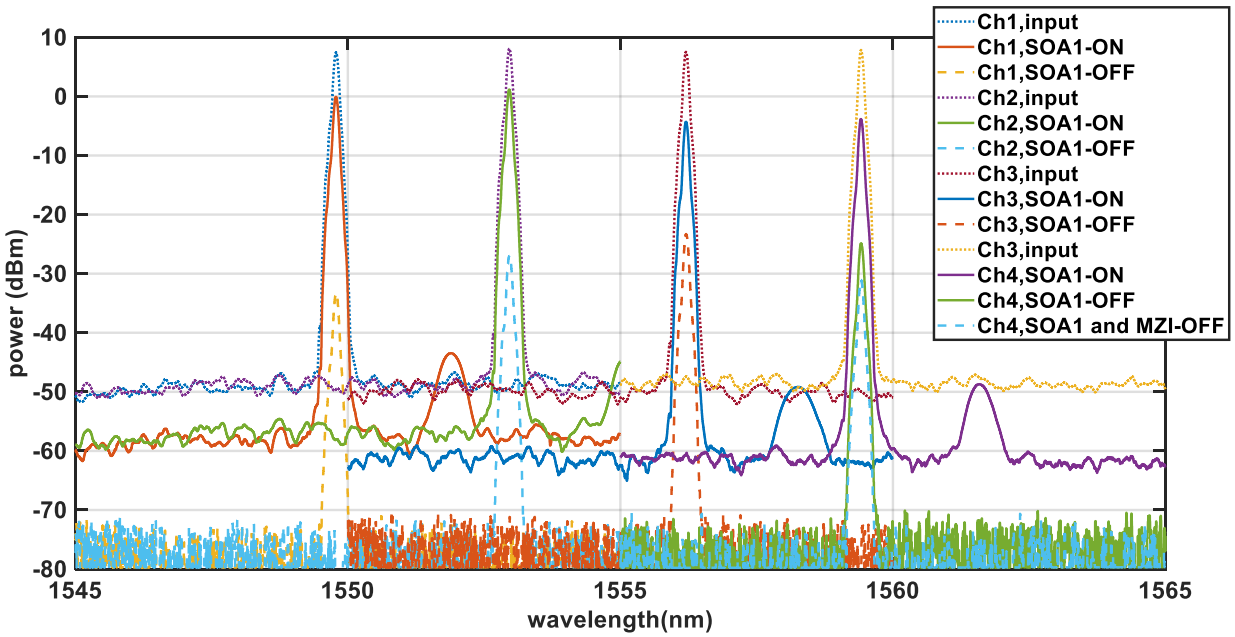


Figure 16 Measured output power of 1x2 WSS, 4 wavelength channels, dotted lines represent input signal. Solid lines represent the WSS output signal when the SOA is in the ON state and the dashed lines represent *the output signal when the SOA is in the OFF state*

multiplexing), and 3 dB MMI splitting loss as well as 5 dB gain generated by the gate SOAs. For Ch3 and Ch4 extra loss of 5 dB is incurred due to the presence MZI switching gates.

These insertion loss values can easily be compensated by incorporating a booster SOA at the input of the WSS which is missing from the current design. On the other hand, an extinction ratio as high as 33 dB (incase of Ch1) is achieved as can be seen in Figure16.

4 SiPh/InP HYBRID WAVELENGTH SELECTIVE SWITCHES

Hybrid wavelength selective switches allow scalable switching capability suitable for high- capacity metro networks due to a superior performance as compared to their monolithic (InP and SiPh) counterparts as they support scalablity to high port and wavelength count. In the hybrid implementation SiPh enables large-scale integration of passive circuitry for demultiplexing and multiplexing while SOAs on InP are used for fast switching functionalities while providing high extinction ratios. In the PASSION project we have implemented the first proof-of-concept hybrid SiPh/InP wavelength blocker (WBL) switching module assembled via flip chip bonding (FCB).

4.1 Design of SiPh and InP PICs

By integrating *m* hybrid WBL modules a 1x*m* hybrid WBLs can be developed. Figure 17(a) shows the schematic representation of a modularly integrated hybrid WSS. It is based on a *broadcast-and-select* scheme, in which the WDM signal is broadcast by a 1x*m* splitter and it is selected by *m* WBL modules at the output ports. A booster SOA on InP dedicated for amplification will be used for compensating the loss of the 1x*m* power splitter. A hybrid WBL with *n*-channels uses 1x*n* deMux/Mux SiPh Arrayed waveguide gratings (AWGs) and *n* SOA switching gates for the *n* wavelength channels. The SOA switching gates are used to pass/block the desired wavelength channel at each of the

output ports. The port count *m* of the WSS is scalable by adding a new WBL switching module. In this presented work, a hybrid WBL module of *n*=12 wavelength channels (10 functional and 2 test channels) with a channel spacing of 0.8 nm (100 GHz) is implemented. The mask layouts of 1x12 AWGs on SiPh and an array of 12 SOA gates on InP are shown in Figure 17(b). The SOA switching gates on InP are placed in a U-shape where the input/output straight waveguides are accessed from the same side. On the SiPh, in addition to deMux and Mux AWGs a cavity is designed for accommodating the InP chip during flip-chip assembly.

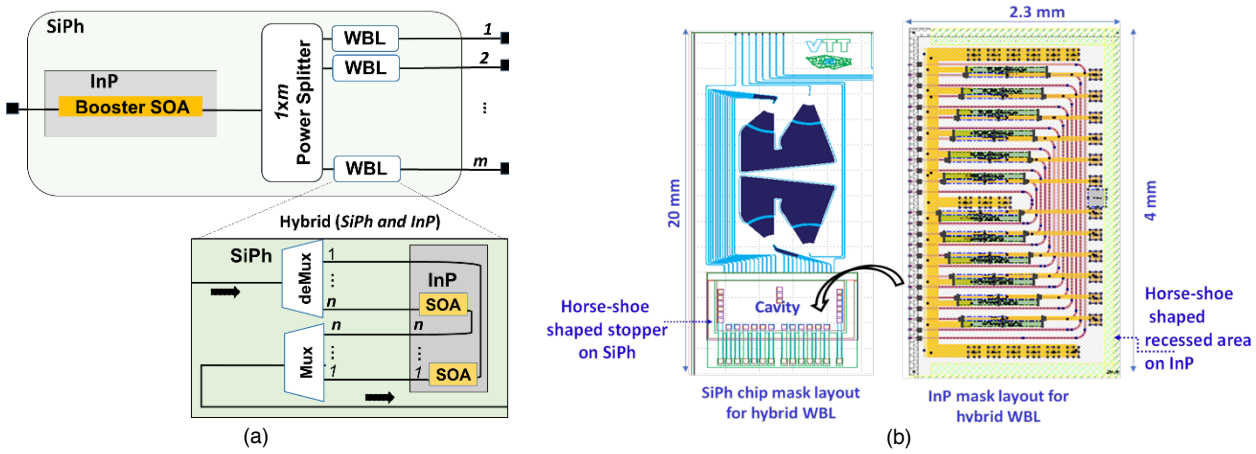


Figure 17 (a)Schematic of modular hybrid integrated wavelength selective switch (b) Mask layout of SiPh passives and zoomed out InP actives

4.2 FLIP-CHIP ASSEMBLY PROCESS

Figure 18 shows the cross-sectional view of hybridly coupled SiPh and InP waveguides. The SiPh waveguide is based on a 3x3 μm VTT's waveguide technology [7] and provides polarization insensitive performance. The InP waveguide is based on a 0.5μm thick waveguide InGaAsP core as shown in Figure 18 (top). Because of the size difference of the two waveguide cores, a tight alignment accuracy of less than ± 0.5 µm in the vertical and lateral directions and an air-gap less than 2 µm between the two waveguides is required to keep hybrid coupling losses below 3 dB. The scheme for FCB assembly process of the hybrid WBL is presented in Figure 18 (bottom). The InP chip is directly bonded with the SiPh cavity via a thermal compression (TC) technique. The Au-coated contact pads of the InP and Sn-coated SiPh contact pads are bonded together with the combined effect of elevated temperature of 220°C and applied bonding pressure. The presence of patterned mechanical stopper (highlighted in Figure 18) on SiPh mechanically supports the InP chip upon FCB. The top contact areas of the SiPh mechanical stoppers and recessed areas in InP chip (highlighted in Figure 17) are lithographically defined to overlap and ensure the self-alignment in the vertical direction.

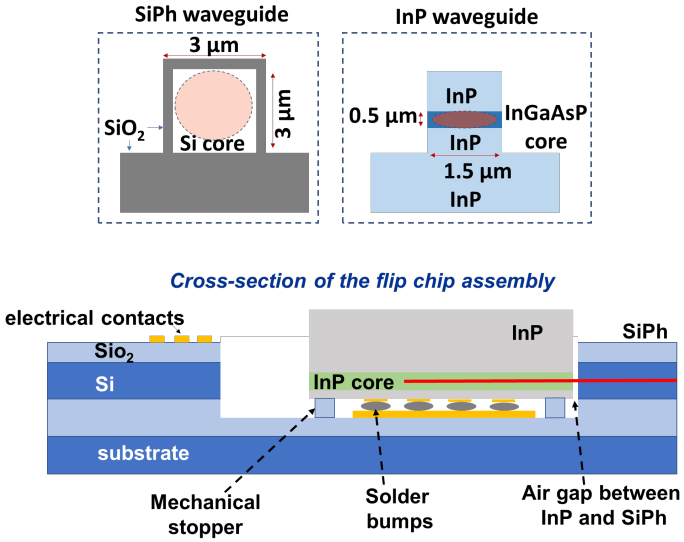


Figure 18 Cross-section of SiPh/InP waveguides (top) and cross-section view of flip chip assembly process (bottom)

Figure 19 shows the photo of the hybrid WBL switch after assembly. Upon FCB, placement accuracy less than 0.5 μm is achieved in the vertical and lateral directions. However, due to limitation in the visual system used for FCB, it was not possible to precisely control the airgap between the two chip

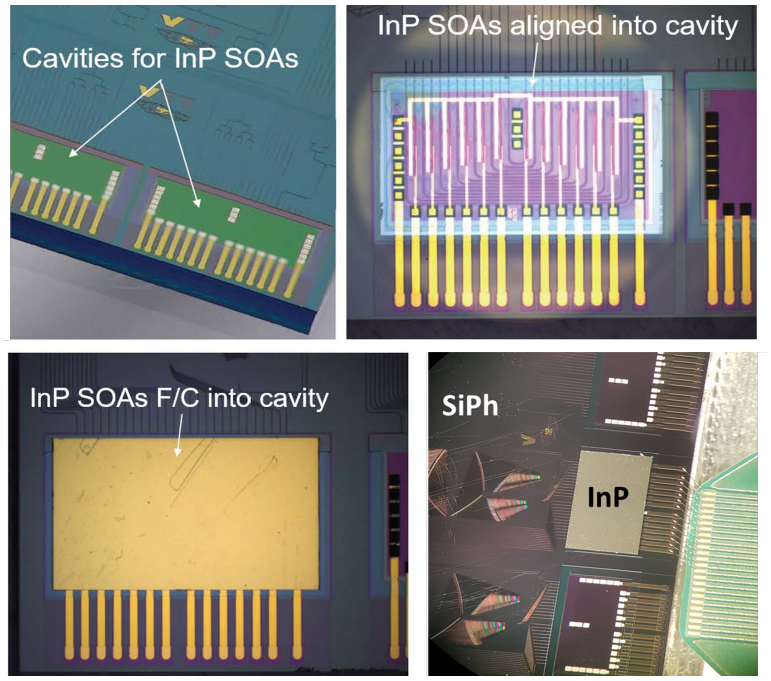


Figure 19 photo of fabricated SiPh chip with cavities (top left), SOA chip aligned into the cavity during FCB (top right), InP chip FCB into cavity (bottom left), hybrid WBL after FCB (bottom right)

facets resulting in an air gap in the order 8 μm; thus leading to excess coupling losses between SiPh and InP. The optimization of the process is ongoing to achieve better performance with respect to this first trial results.

4.3 CHARACTERIZATION RESULTS

At first, the hybrid WBL is electrically and optically characterized. Out of the 10 wavelength channels, 8 channels Ch1, Ch3,…,Ch9 are working and were characterized optically and electrically. Next data transmission tests at 10 Gbps and 20 Gbps NRZ data rate were conducted. Figure 20 shows the I-V curve of the SOA gate switches before and after FCB assembly. Comparing the I-V curve before and after integration, only a variation of 4.5 Ohms in resistance is observed. Next, the 3-dB bandwidth of deMux and Mux SiPh AWGs was measured as 50 GHz and it matches the design specification. It was further observed that the deMux/Mux AWGs have a good central wavelength channel matching; for instance, Ch7 has a relative shift of only 0.07 nm between deMux and Mux as illustrated in Figure 21. Figure 22 shows transmission characteristics of eight wavelength channels when the SOA gates are On/Off for an input optical power of 0 dBm. Solid lines represent the WBL output when the gate SOA is *On* state and the dashed line shows the WBL output when the gate SOA is in the *Off* state. The typical measured On/Off ratio is around 30 dB. The fiber-to-fiber losses for Ch1, Ch3, Ch6, Ch7, Ch8 range from 32.2 to 37.5 dB. The current for each gate SOA is optimally tuned to minimize both the fiber-to-fiber loss and the effect of back reflection on the hybrid WBL. Accounting for 2.5 dB insertion loss per AWG and 3 dB/facet for chip-to-fiber coupling losses, 3 dB gain of the SOA at 40 mA, the best channel (Ch3) has 12 dB/facet hybrid coupling loss: resulting excess loss of 9dB/facet. We believe the measured excess losses are the result of tight alignment tolerance which can be improved by reducing the air-gap (now in the order of 8μm); additionally, it can be relaxed by using on-chip integrated spot-size converters (SSC). In our future implementation,

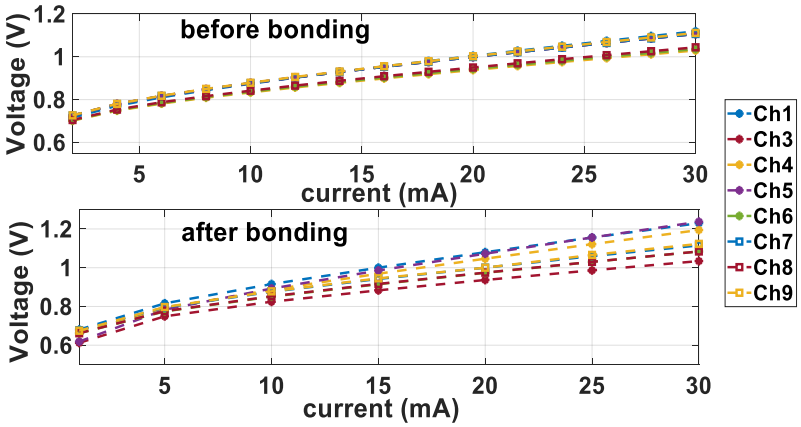


Figure 20 I-V curve of the SOAs before and after flip-chip bonding

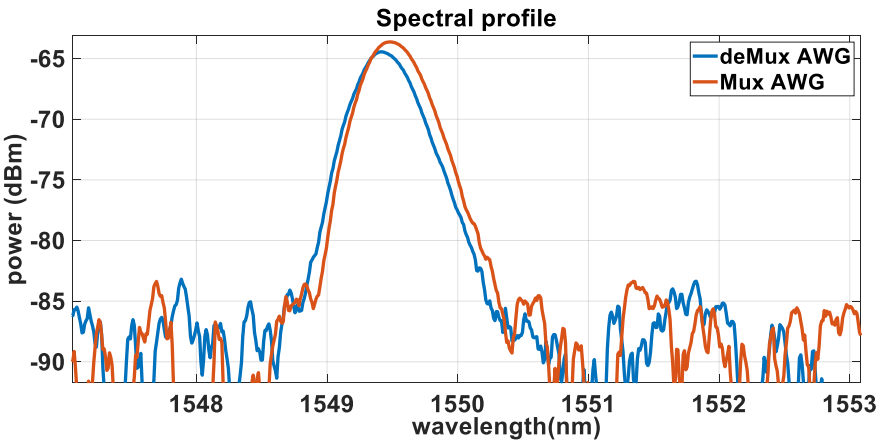


Figure 21 AWGs spectral profile, collected ASE (SOA) from Ch7

we also plan to use angled waveguides to alleviate the impact of back reflection and fully employ the gain of SOAs. Figure 23 shows the gain characteristics of the gate SOA for Ch3 for varying current and varying input power. It is shown that fibre-to-fibre loss varies from 60 dB at the absorption state of the SOA at 0 mA to 26 dB due to the gain provided by the SOA at 100 mA. The fibre-to-fibre loss is in the order of 33 dB at 80 mA for all input power values. The loss decreases to 26 dB at SOA current of 100mA; for input power of 0 dBm and -5 dBm. Effects of SOA saturation on the fibre- to-fibre loss is slightly observed at 100 mA for input power of 7 dBm and 10 dBm resulting fibre-to-fibre losses of 29 dB and 31.57 dB respectively. Table.3 summarizes the fibre-to-fibre loss of each channel, and the corresponding current of the SOA gate.

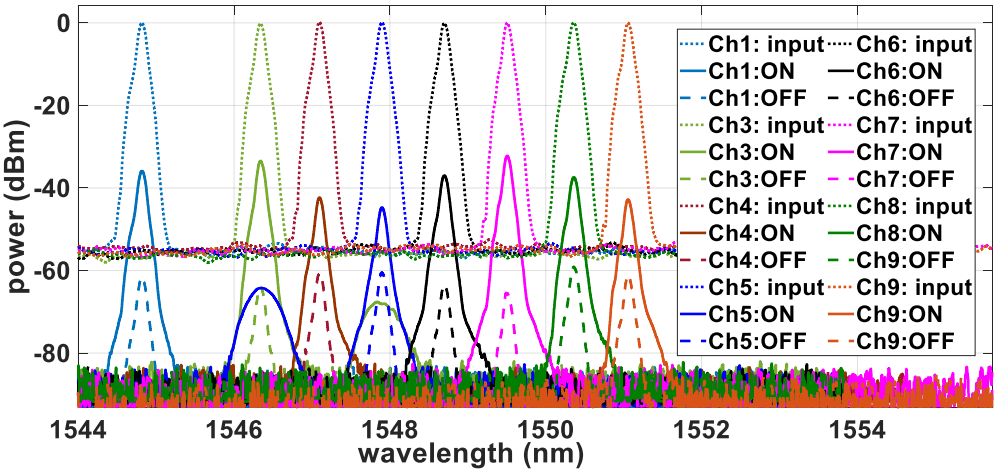


Figure 22 Input optical signal (dotted line), output optical signal of the Hybrid WBL switch ON (solid line) /Off state (dashed line)

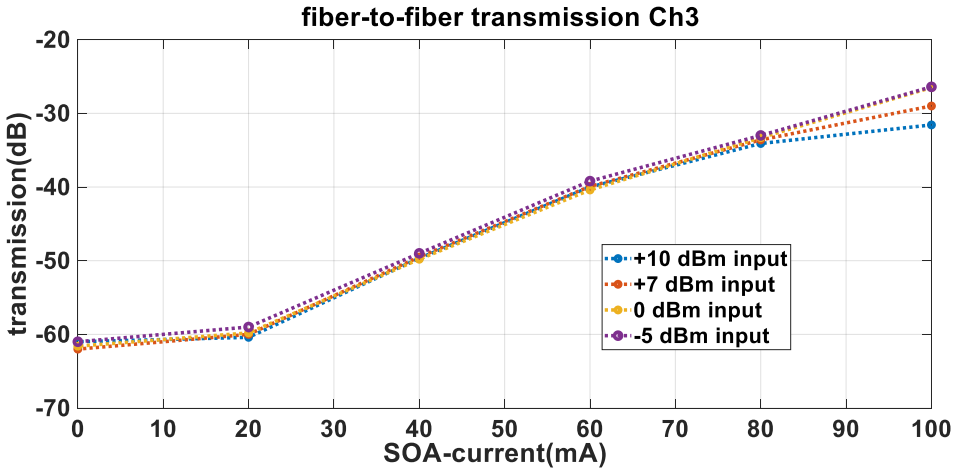


Figure 23 fiber-to-fiber transmission and gain characteristics of SOA (Ch3)

Table 3 Fiber-to-fiber insertion loss

Channel number	1	3	4	5	6	7	8	9
Fiber-to-fiber loss (dB)	36	33.4	42.3	44.8	37.0	32.2	37.5	42.8
SOA current (mA)	40	80	80	80	90	40	80	28

4.4 DATA TRANSMISSION

Figure 24 shows the experimental setup for the data transmission through the hybrid WBL. A tunable laser source is used to generate light for wavelengths corresponding to the channels of the WBL. Lensed fibers are used to couple light in/out of the hybrid WBL switch. The input optical modulated signal was boosted to 17 dBm to compensate the losses in the hybrid WBL. After transmission through the WBL, the output signal is variably attenuated before being input to the receiver.

4.4.1 NRZ data transmission at 10 Gbps

A 2^7-1 NRZ 10Gbps data is externally modulated and transmitted through the hybrid WBL switch and detected at the receiver (highlighted as link *a in* Figure 24). Figure 25 shows the BER measurements of five channels Ch1, Ch3, Ch6, Ch7 and Ch8 at 10 Gbps 2^7-1 PRBS NRZ data. Error free transmission is obtained with power penalties ranging from 0.3 dB to 1.5 dB. Clearly open eye diagrams of the five channels are obtained as shown in Figure 25.

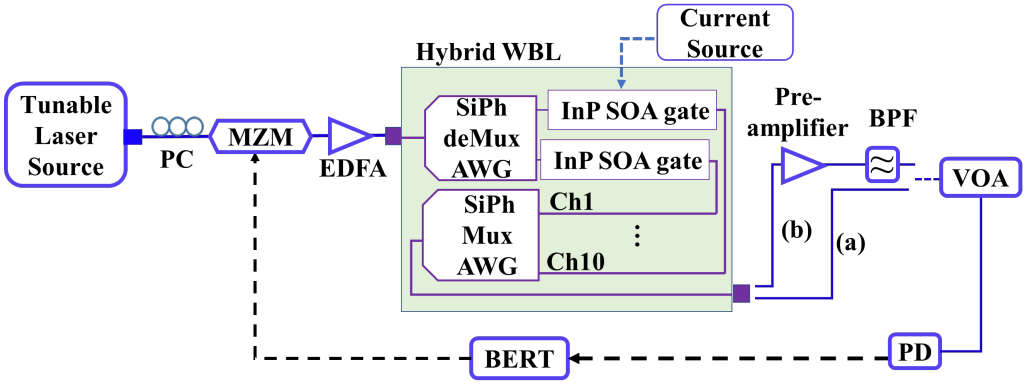


Figure 24 Experimental setup for NRZ data transmission (a) 10 Gbps without pre-amplifier *(b) 20 Gbps with pre-amplifier and bandpass filter (BPF)*

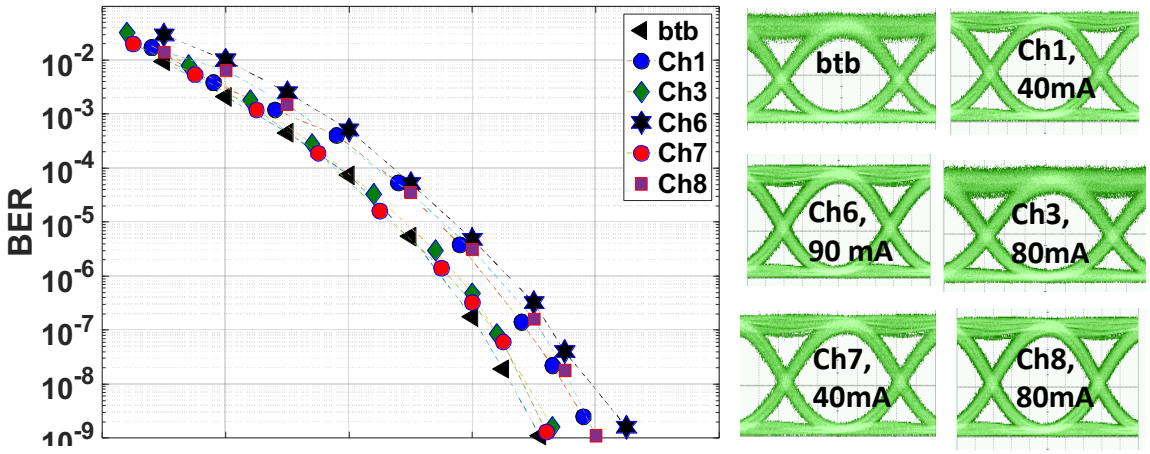


Figure 25 BER vs received power at 10 Gbps NRZ

4.4.2 NRZ data transmission at 20 Gbps

For the transmission of 20 Gbps 2^{31}-1 NRZ data through SiPh/InP hybrid WBL switch the setup illustrated in Figure 24 is used. After the transmission through the WBL, a second preamplifier (highlighted in *link (b)* in Figure 24) is used to reach the sensitivity of the 20 Gbps receiver. A bandpass filter (BPF) with 3 dB bandwidth of 200 GHz is used before the receiver. Error free transmission is achieved for Ch1, Ch3, Ch6, Ch7, and Ch8 as shown in Table. 4. The penalties range from *0.7 dB* in case of Ch3 to *2.8 dB* in case of Ch8 at BER of *1E-9*. The current of the SOA for each channel is optimized to minimize power penalties. Figure 26 shows the plot of BER vs received power for 20 Gbps transmission for two channels (Ch3 and Ch7) and the open eye diagrams of the five channels. These successful data transmissions performed on the first proof-of-concept modularly designed hybrid WBL verify its feasibility to be used in high capacity metro-core switching node where capacity can be scaled by adding new modules in a pay-as-you-grow manner.

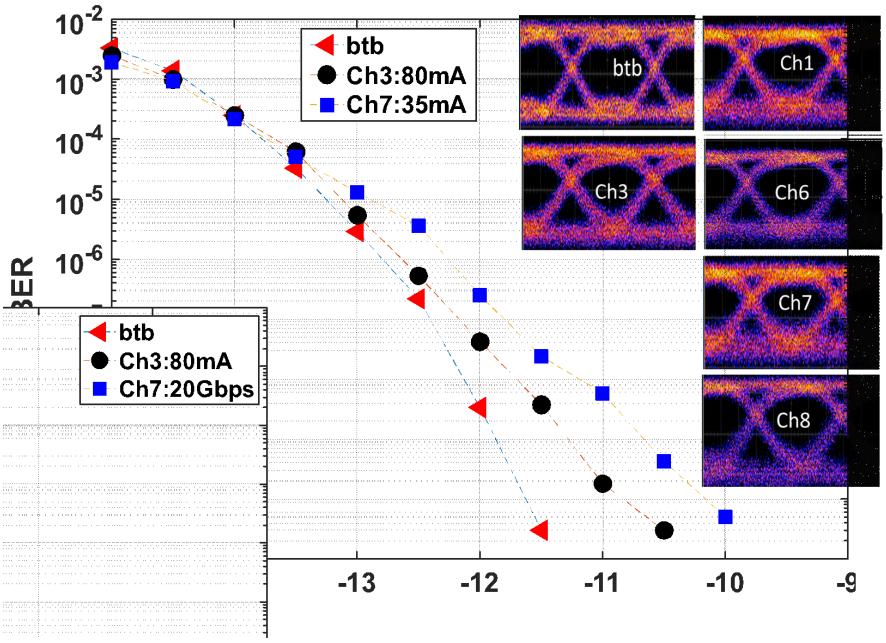


Figure 26 BER vs received power at 20 Gbps NRZ

Table 4 power penalty @ BER 1e-9 for 20 Gbps transmission

Channel	Ch1	Ch3	Ch6	Ch7	Ch8
Penalty (dB) at 1E-9	1.3	0.7	2	1.4	2.8
Current (mA) of SOA	35	80	90	35	60

This first trial assembly process is followed by on-going efforts to reduce excess hybrid coupling losses via optimization of the flip-chip assembly process, the use of on-chip spot-size converters to relax tight alignment tolerances, and by employing angled waveguides at the facets to reduce back reflections.

The demonstrated error free transmission of 10 Gbps and 20 Gbps per wavelength channel opens to scalable switching functionality, which is pivotal for next generation modular metro-networks

5 CONCLUSIONS

In this deliverable, the characterization of the realized on-chip switches both on monolithic InP and hybrid SiPh/InP platform is presented. Two type of switches are realized. The first one is a wavelength selective switch (WSS), that involves switching one or more wavelength channel at the input port to any output port, and the second one is a multi-cast switch (MCS) involving the switching of an input signal to multiple output ports irrespective of wavelength. The selection of the desired wavelength channel is accomplished at the coherent receiver module.

A 2x4 MCS module on InP that provides connectivity between two input ports and 4 output ports was realized. The MCS is based on a *broadcast and select* topology. A 2x4 splitter followed by a network of waveguide crossings is used to distribute the copies of the input signals to the four output ports. A selection stage constituted by 2 SOA gates and 2 by 1 power combiners is implemented at each of the output ports. A booster SOA at the input port is used to provide gain for compensating on-chip splitter and combiner losses. Characterization results show a lossless performance through multiple paths through the MCS and output signal with high OSNR values.

The functionality of a compact 4-channel 1x2 WSS module on InP based on a single 3 x12 AWG was demonstrated. The design reduces the device footprint by reducing the number of required AWGs by three. Insertion loss values of 7 dB and cross-talk level of 33 dB is achieved. The insertion loss could easily be compensated by introducing a booster SOA into the design.

A SiPh/InP hybrid wavelength blocker switch was realized via flipchip bonding assembly of SiPh AWG demultiplexer/multiplexer passives and InP SOA active switching gates. The obtained hybrid SiPh/InP waveguide coupling losses can be improved by incorporating on-chip spot size converters to relax the tight alignment tolerance. By compensating the device insertion loss with an optical preamplifier successful data the transmission of 10 Gbps and 20 Gbps NRZ data was demonstrated through the hybrid WBL.

These reported measurement results of the on-chip switching functionalites validate the fact that the realized switching modules can be deployed in PASSION's high capacity metro switching nodes. Scalablity is supported in which switching modules are added in a pay-as-you grow manner in response to capacity increase. The presented switching node architecture is geared to maximize network efficiency and optimize uitilization of resources which is instrumental in the next generation metro networks.

6 ACRONYMS

ASE	Amplified spontaneous emission
AWG	Arrayed waveguide grating
BER	Bit error rate
BPF	Band pass filter
dB	Decibel
dBm	Decibel-milliwats
FCB	Flip chip bonding
InP	Indium phosphide
MCS	Multi cast switch
MZM	Mach-zehnder modulator
MZI	Mach-zehnder interferometer
NRZ	Non return to zero
OSNR	Optical signal-to-noise ratio
PIC	Photonic integrated chips
PRBS	Psuedo random beat sequence
PS	Power splitter
SDN	Software defined network
SiPh	Silicon Photonics
SOA	Semi-conductor optical amplifier
SSC	Spot-size converters
TC	Thermal compression
WBL	Wavelength blocker
WDM	Wavelength division multiplexing
WSS	Wavelength selective switch

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