D3.7 Test results from the full Tx modules

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TABLE OF CONTENTS

TABLE OF FIGURES

EXECUTIVE SUMMARY

This report provides a detailed description of the design, fabrication and testing of the full transmitter (Tx) module (MOD) developed in the PASSION project to target up to 2-Tb/s capacity.

A significant progress has been achieved compared to D3.4 in the packaging and assembly of the vertical cavity surface emitting lasers (VCSELs) on top/below the silicon photonics (SiPh) photonic integrated circuit (PIC) delivering good coupling losses and first demonstration of wavelength division multiplexing (WDM) operation of combined VCSEL+PIC module. The development of the VCSELs has continued and the required tuning through current variation has been proven to be a viable route towards the modular PASSION approach adopted to build the fully-equipped super-MOD targeting up to 16-Tb/s capacity. Same VCSELs were also demonstrated to support the required single channel bit rate (50 Gb/s per VCSEL per polarization) and beyond.

Major progress on the complete packaging of the SiPh chip into a functional Tx MOD, with accompanying hardware (HW) and software (SW) were conducted resulting in a fully deployable TX module.

Due to issues with the fabrication of the printed circuit board (PCB) connecting the PIC to the evaluation board, the full module could not be completely tested. Since these issues are not due to the technology developed in the PASSION project but are related to a production failure of a mature component such as the PCB, we confirm that the developed Tx module demonstrates the PASSION concept and we provide proof of the effectiveness of the PASSION technologies.

1 INTRODUCTION

This report will provide a detailed description of the design, fabrication and testing activities which were taken in order to confirm the proper operation of the PASSION Tx MOD concept. The details concerning the design considerations for the VCSEL and the SiPh PIC have been included in the deliverable *D3.1 Detailed design of the Tx module architecture and interfaces*. Information concerning the light coupling from VCSEL to SiPh PIC are included in the deliverable *D3.4 Test results from passive SiPh PICs integrated with VCSELs* and additional information of the Tx module design are included in the deliverable *D3.6 Test results from the first transmitter submodule with directly modulated VCSELs*.

The assembly of the Tx module needs to address several different technological challenges. These include but are not restricted to:

- The optimal coupling of light from the large aperture of the VCSEL into the relatively narrow waveguides and the associated losses incurred or remedies which can be offered to overcome these losses.
- The proper electrical wiring (metal traces) needed to carry high speed signals from the VCSEL drives (See D3.1 & D3.2) to the VCSEL with maximal fidelity on top/bottom of the SiPh chip.
- The thermal conditions in which the VCSEL are operating depending on their position relative to the SiPh waveguides.
- The tuning mechanism of the VCSELs under current injection variations.
- The high-speed operation of VCSELs in combination with the drivers provided by IDT.
- The assembly and packaging of the SiPh PIC into the complete Tx module.
- The design of the PCB interposer to fan out signals from the PIC to the evaluation board (EVB).
- The co-integration of the PIC with the PCB interposer and mounting on the EVB.

After a detailed overview of the activities leading to the assembly of the passion Tx MOD in Section 2, we report in Section 3 on the most recent results concerning the coupling between VCSEL and SiPh obtained in the last year of the project and the most recent data concerning the VCSEL fabrication and operation. In Section 4 the experimental tests of the full Tx MOD technologies as well as data on partial testing is included.

2 PASSION TX FINAL MOD ASSEMBLY PROCESSES

In this section we describe the PASSION Tx final MOD assembly process, highlighting the critical processes, equipment and evaluation boards used.

2.1 TX MOD ASSEMBLY FLOW CHART

The Tx MOD transmitter assembly has been conceived as a number of preparatory, assembling, visual inspecting, merging, closing, sealing and testing phases.

Whether possible a parallel execution approach has been privileged, such as kit-create and component-lots preparation, VERT VCSEL selection for ITU channel mapping on PIC, passive

components (resistors, capacitors and inductors) surface mounted (SMD) on the interposer, solder-bumping of the Interposer for VCSEL drivers flip-chip assembly, etc.

A simplified assembly flow chart is depicted in Figure 1 showing the most relevant assembly phases. Each described assembly block includes several visual inspection and cleaning processes.

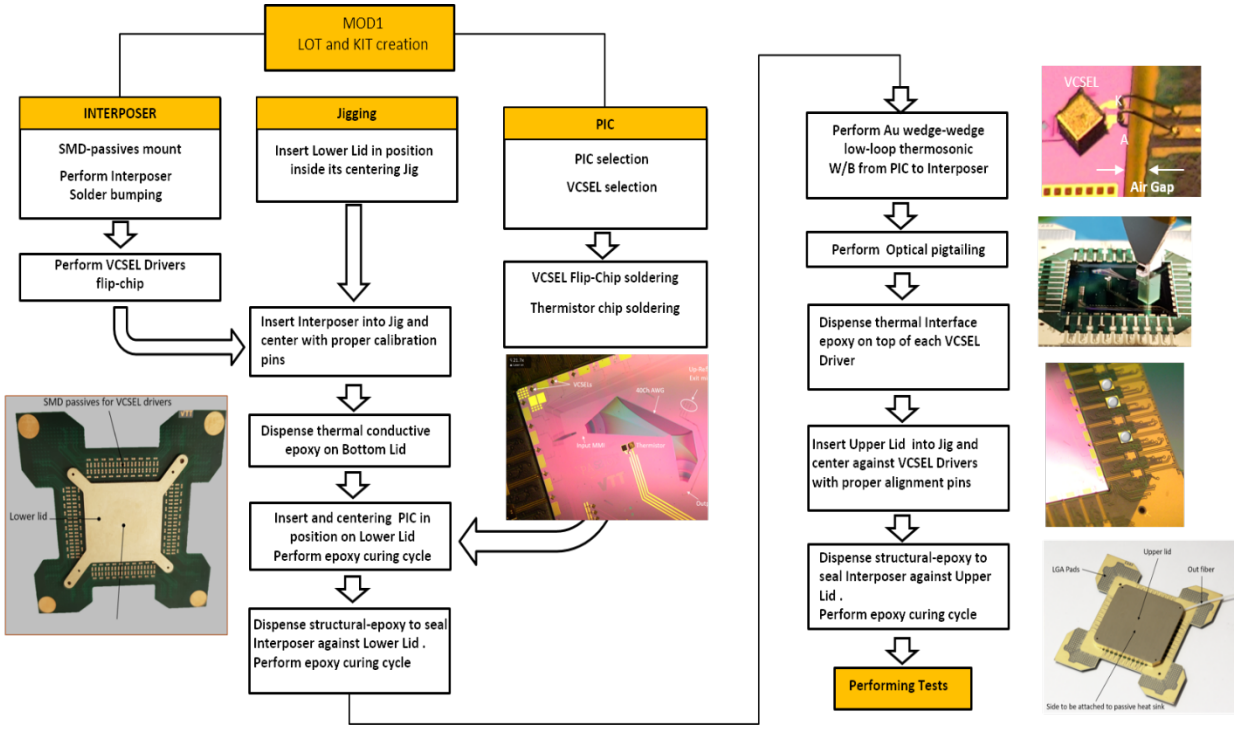


Figure 1. MOD simplified assembly flow chart.

2.2 TX MOD FIBER PIGTAILING PROCESS

Before to proceed with thermosonic wirebonding, the output fibre pigtail on PIC has to be performed. This is a delicate step and can be carried out in two ways as described below:

1) When the PIC is fully populated with 40 VCSELs, as in case of the PASSION full Tx MOD, then an external set-up electrically probes the PIC powering a selected VCSEL. A high precision current source (e.g. Keithley 2401 or 2450) is needed to drive the VCSEL to a specific bias current point in a way to tune the wavelength to a corresponding ITU channel and passing through the arrayed waveguide grating (AWG). The light collected at the output

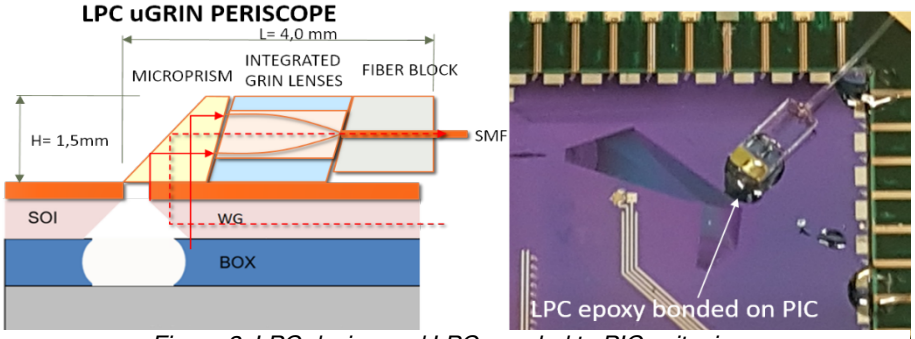


Figure 2. LPC design and LPC coupled to PIC exit mirror.

mirror is then coupled into a single mode fibre (SMF) through a micro-GRIN periscope pigtail assembly (LPC) as shown in Figure 2.

2) The remnant fibre end is then connected to an optical power meter. A high resolution (<10nm) piezoelectric alignment engine provides accurate positioning to maximize the coupled optical power. A small amount of index-matching UV epoxy (Norland NOA61) is then dispensed in proximity of the LPC- PIC interstitial air gap and left to rapidly spread for capillarity. After possible small re-alignments to maximize again the coupled power, a 365nm curing beam (irradiance approx.180mW/cm^2) is then addressed to the epoxy and surrounding area for approx. 1 minute to complete the curing process and terminate the pigtailing phase.

3) In case the PIC is partially populated with VCSELs, then few ITU channel mirrors may result available and suitable for launching optical signals at their specific wavelengths. In this case a lensed SMF designed to match the same mode field diameter (MFD) of the PIC waveguides (2.8 μm) is positioned and coupled on top of any available mirror (Figure 3). The remnant end of the fibre is connected to a broadband source (e.g. amplified spontaneous emission (ASE) or super luminescent diode (SLD) sources with 80nm BW) in a way to cover any

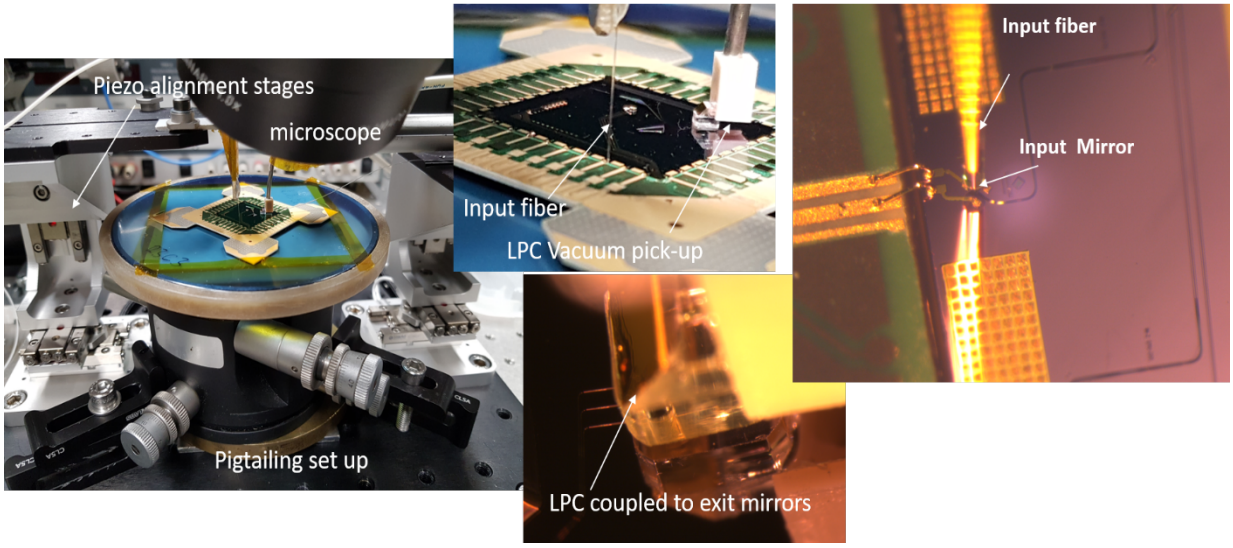


Figure 3. (Left) Pigtailing bench set up and (Centre to Right) Lensed Input fiber and LPC pigtailing.

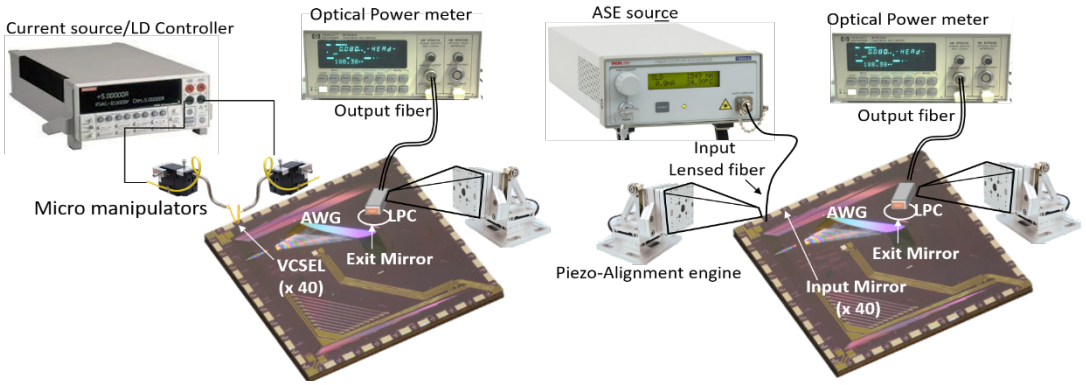


Figure 4. PIC to fibre alignment strategy. (Left) Power-up any VCSEL on PIC with micro-manipulator probes or (Right) launching light with a broadband source (eg.80nm) to any available input mirror through a lensed fibre matching the 2.8μm MFD of the SOI waveguide.

wavelength multiplexed by the AWG. Two high resolution (<10nm), 3-axis piezoelectric alignment engines, provide accurate and independent launching fibre and LPC positioning on respective mirrors. The procedure to maximize the output power is then the same described in point 1. A schematic diagram of the two alignment approaches are depicted in Figure 4.

2.3 Tx MOD Evaluation Board

In this section we describe the EVB designed to host and interconnect the Tx MOD to all needed power supply lines, I2C control interface, RF input connectors and optical output fibre, with the aim to perform initial E/O characterization before to be moved into the real industrial platform based on LM1-WDM/LM1-OTN products such as those developed in PASSION by partner SMO (as described in deliverable D3.6). The EVB has been designed to independently control each single VCSEL driver and it requires a rigid chassis to maintain a flatness in the Tx MOD contacting area of <50μm². The

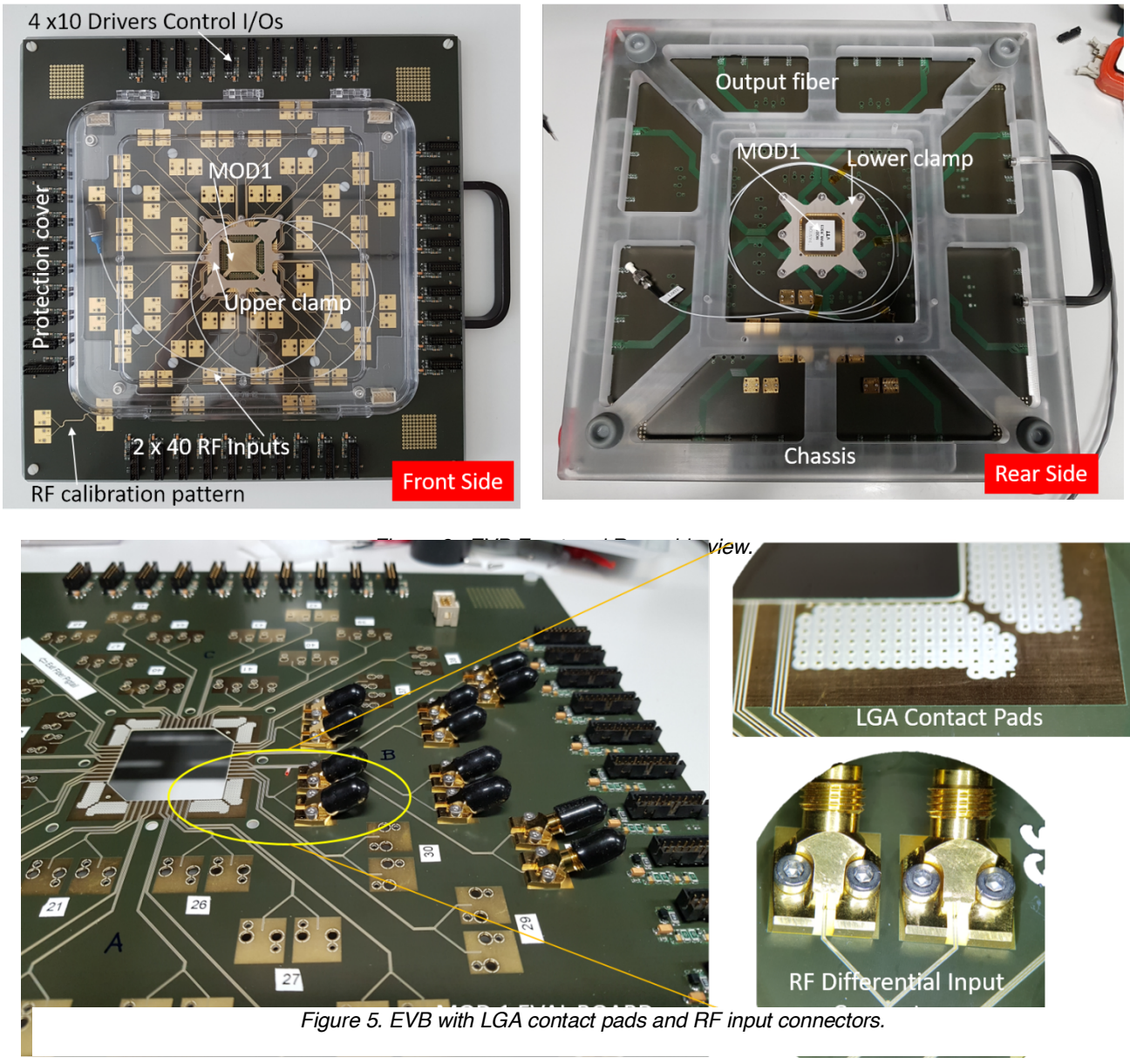


Figure 5. EVB with LGA contact pads and RF input connectors.

position of the 2 x 40 RF connectors (Rosenberger 08K80F-40ML5) reflect the 10 x 4 ITU channels disposition on the Tx MOD (Figure 6 and Figure 5).

2.4 ELECTRICAL DIAGRAMS

In the Tx MOD development two main electrical schematics have been designed to provide all electrical services and interconnections required for VCSEL Driver HXT14100.

One refers to the essential critical components that must stay close to the driver, in particular 5 by-pass capacitors which are responsible to filter direct current (DC) lines from RF noises inside the driver, as shown in Figure 7. Such arrangement has been then replicated 40 times as the maximum number of channels available in the Tx MOD.

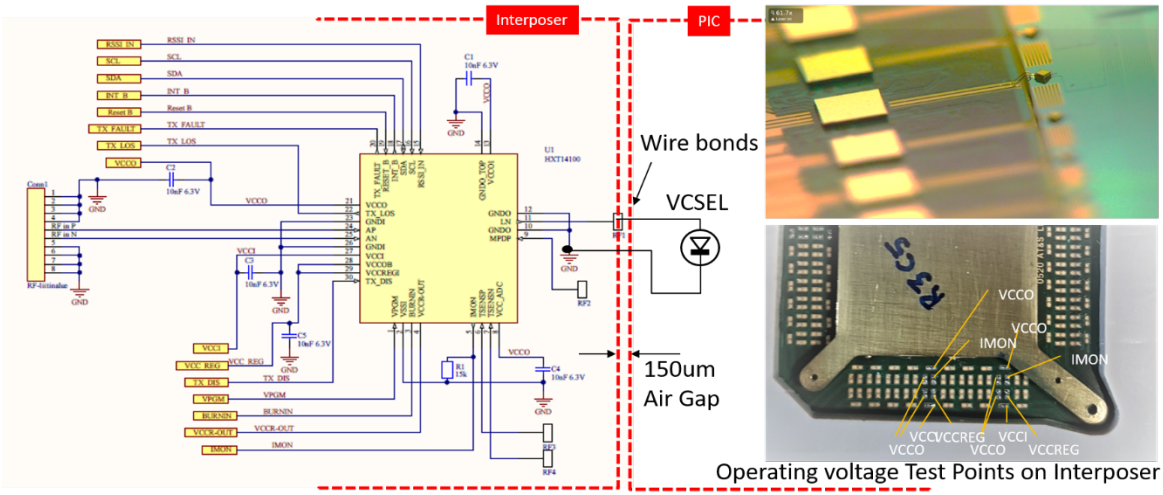


Figure 7 HXT14100 VCSEL Driver Electrical diagram on the Tx MOD.

The second refers to remnant interconnections including I2C lines, additional DC voltage splitting and filtering, wholly available through a single 20pin I/O connector. Due to the bulky physical

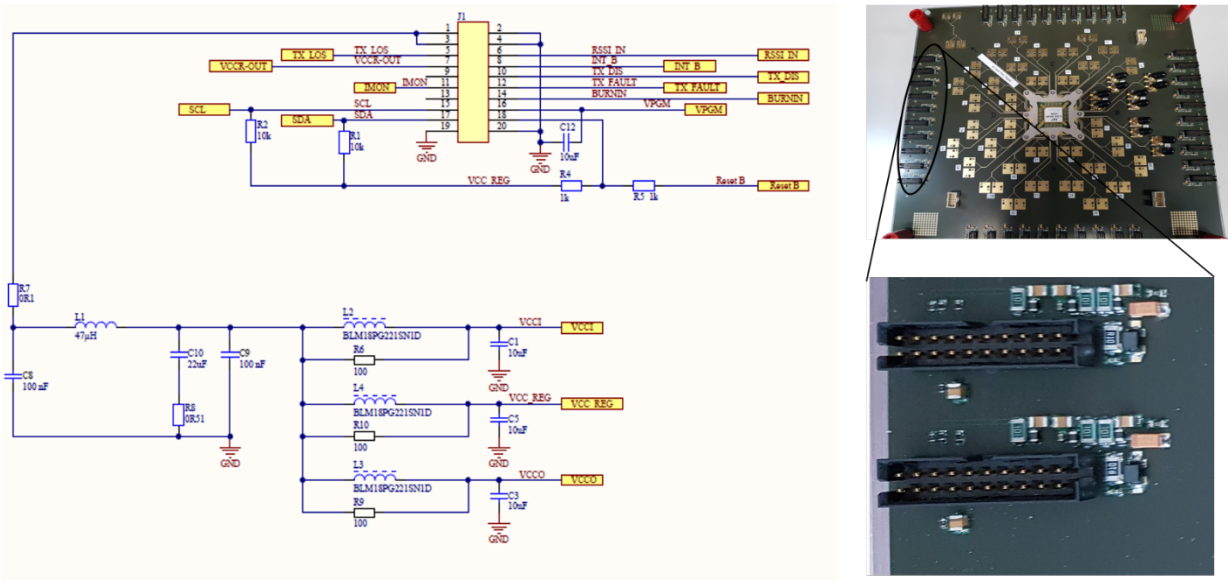
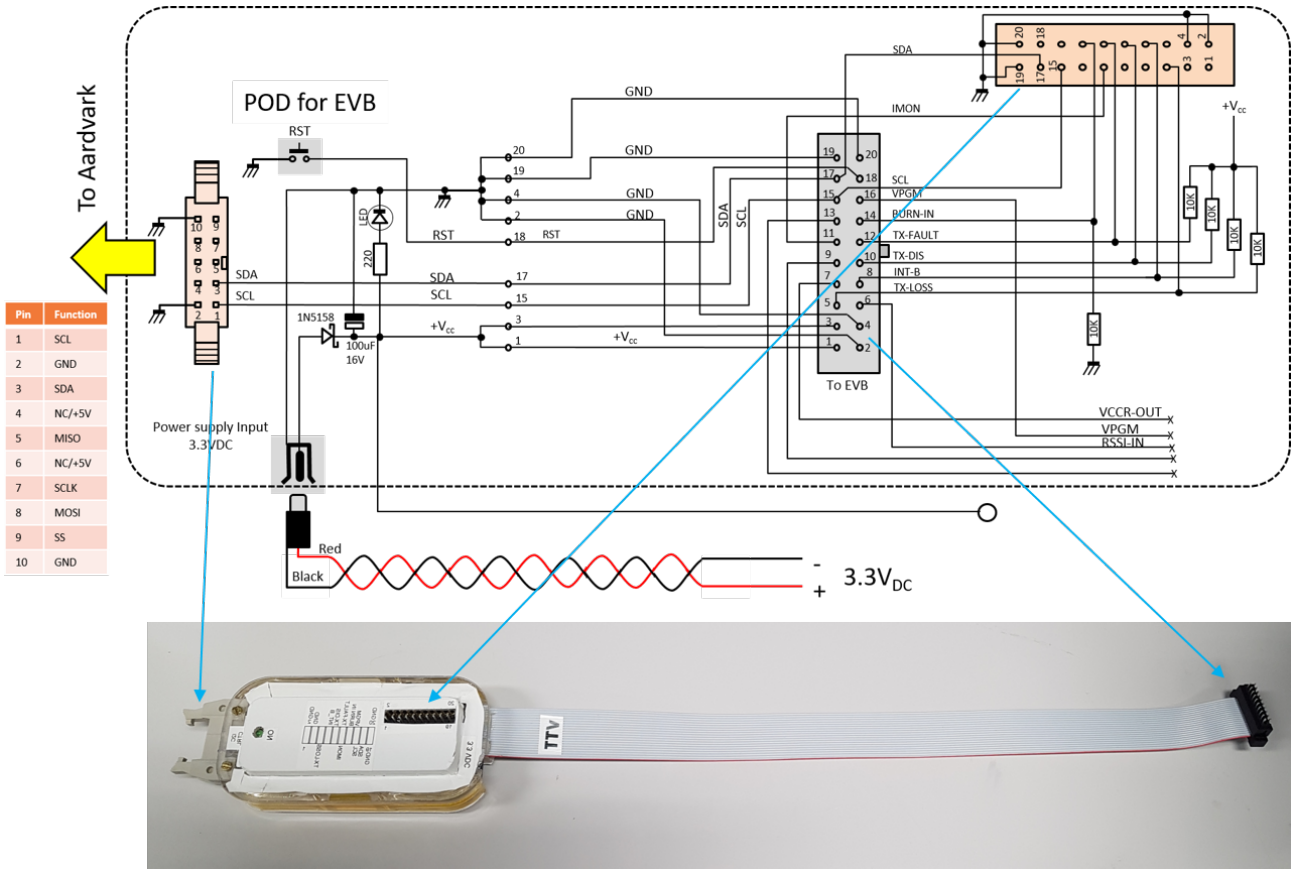


Figure 8. EVB Channel connector to address all needed power supplies and I2C control interface to a corresponding VCSEL driver on MOD1. On EVB there are up to 40 independent channel connectors.

dimensions of the additional needed components (more capacitors, resistors and inductors) this electrical part has been conveniently embedded into EVB and shown in Figure 8. Again, this approach has been then replicated 40 times as the maximum number of channels available for the Tx MOD.

The availability of a single I/O connector per channel greatly simplify functional tests of every VCSEL on the Tx MOD. However, to reduce the number of cables and wiring during testing a small additional utility-box (POD2) has been designed with the purpose to make easy interconnections toward I2C controller (Aardvark-TotalPhase), computer, and main power supply (Figure 9).



Pin	Function
1	SCL
2	GND
3	SDA
4	NC/+5V
5	MISO
6	NC/+5V
7	SCLK
8	MOSI
9	SS
10	GND

Figure 9. Utility box POD 2 for I2C to Aardvark computer interfacing and to EVB.

2.5 Tx MOD E/O Testing

A set of 4 Tx MODs have been assembled with a relatively small amount (2÷6) of VCSELs mounted for initial performing tests. Finally, 2 more MODs embedding MPW9-R3C3 and MPW9-R2C4 PICs, have been populated with 20 and 21 VCSELs, respectively (Figure 10).

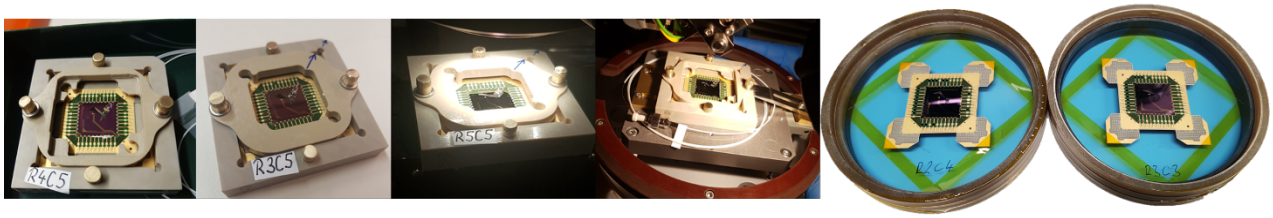


Figure 10. All manufactured MODs under their assembly jigs.

2.6 Tx MOD Channel Mapping Approach

Several VCSEL batches provided by the PASSION partner VERT allowed to largely populate both MPW9-R3C3 and R2C4 modules. Two VCSEL distribution maps have been defined in a way to evenly distribute the available lasers between the two MODs and maximize the ITU channels´ coverage allowing a broader set of systemic performing tests. Both VCSEL distribution maps are shown in Figure 11.

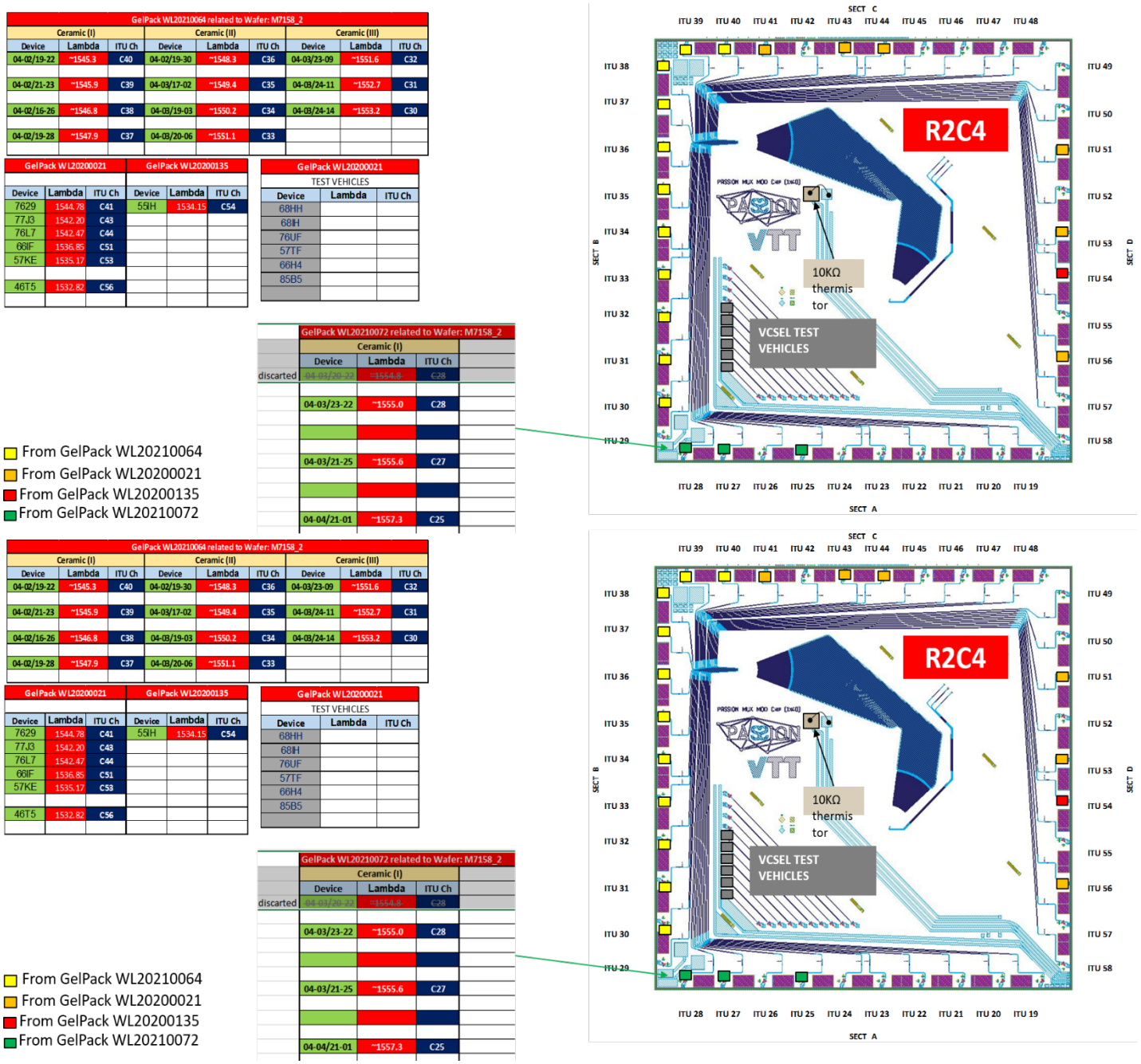


Figure 11. MOD MPW9-R3C3 VCSEL and ITU channel map.

When allocating each VCSEL on the PIC to the respective ITU channel, the estimated wavelenght has been calculated considering the needs to exploit the maximum modulation bandwidth at the specific operating wavelength, which varies as a function of I_{bias} of approximately 0.3 nm/mA, as also anticipated in the deliverable D3.6. We calculated the maximum modulation bandwidth having the I_{bias} to satisfy the following relation $\sqrt{I_{bias} - I_{th}}$= 2.5/3. Maximum bandwidth is achieved at I_{bias} of about 8-8.5 mA, corresponding to $(I_{bias}-I_{th})^{0.5}$=2.74 (I_{th}=1 mA), as reported in Figure 12.

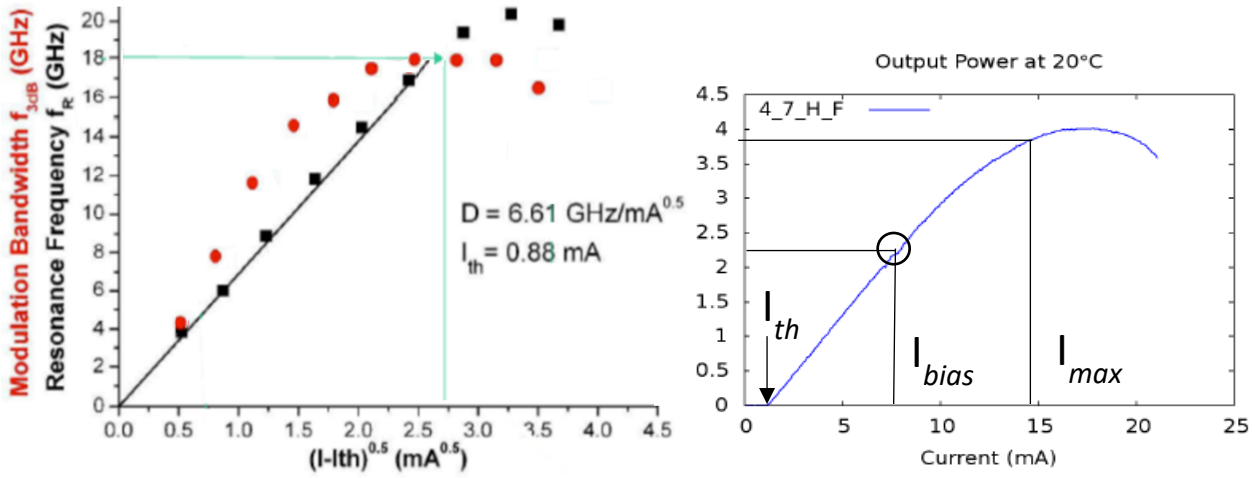


Figure 12. Modulation bandwidth (red circle) and resonance frequency (black square) as a function of the I_{bias}. Maximum bandwidth is achieved at I_{bias} of about 8.5mA, corresponding to $(I-I_{th})^{0.5}$=2.74 (having I_{th}=1 mA).

3 CO-INTEGRATION OF VCSELS AND SIPH PIC

In this section we describe the steps taken in order to accomplish the co-integration of the VERT VCSELs and the VTT SiPh PIC. Next to the details of the assembly and fabrication steps related to the top illumination approach in Section 3.2 (selected as primary strategy in the project), we will also give details of results of the alternative approach which aims to use bottom illumination in Section 3.3.

3.1 VCSELS DESIGN AND FABRICATION CHOICES

In PASSION project, the VCSEL devices are developed and produced by the partner VERT with the following targets/results achieved:

- Single-mode operation;
- low power consumption < 35mW
- output power about 4 mW @ 20°C
- achieved bandwidth S_{21} = 15 GHz (20GHz theoretical bandwidth limited by parasitics)
  - 50 Gb/s rate per VCSEL thanks to direct discrete multitone (DMT) modulation
- layout optimized for flip chip bonding
- far field FWHM < 15°
- SMSR > 35dB
- low threshold current I_{th} < 2.5 mA @ 20°C

VERT further developed the VCSEL design and process technology to realize VCSELs with the necessary parameters and performance to meet the PASSION requirements. One key focus was to provide VCSELs that cover the wavelength span of the C-band ITU channels from Ch 19 (1562 nm) to CH 59 (1530nm). During the project, VCSELs were produced from 1530 nm to 1562 nm and project partners have been sampled with a significant number of VCSELs to develop test setups and integrated solutions for these ITU channels. A VCSEL design platform, based on a short cavity design with two dielectric distributed Bragg reflectors (DBRs) and short resonator, has been developed for both 2" and 3" wafers that are being produced in different epitaxy equipment. The 2" platform provided some advantage to cover a wider range of VCSEL wavelengths on one wafer, as the epitaxy has a larger inhomogeneity and allowed to realize a wider wavelength variation. As such it has been achieved to realize VCSELs from below 1530nm to 1562nm on one wafer. The VCSELs showed excellent single mode behavior, with a SMSR exceeding 40 dB and providing an optical power of up to 5mW at 30°C and 2.5 mW at 70°C.
The bandwidth with up to 15 GHz (S21 3dB) provided very good performance to achieve the target 50-Gb/s transmission rate thanks to DMT modulation. The VCSEL design was optimized for a theoretical performance of 20 GHz, but was limited by parasitic parameters. In the future, these parasitic parameters will be further reduced.
A very important aspect of the VCSELs is the wavelength tuning by bias current. The VCSELs can be tuned to the required ITU channel by temperature controlling the center wavelength and subsequently tuning the laser by adjusting the bias current. The VCSELs feature a tuning range of ca. 3.5 nm from 5 to 15 mA (see Figure 13 (right)).

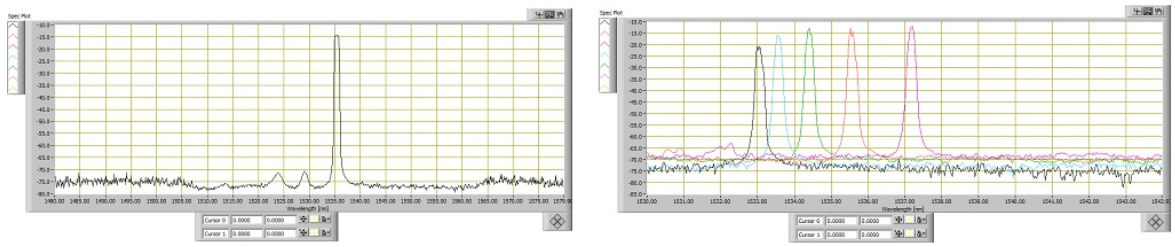


Figure 13. (Left) Spectrum and SMSR of VCSE; (Right) Wavelength tuning.

The figure below shows the excellent optical power performance from -10°C to 80°C, as well as the low power dissipation with a typical operating voltage of below 1.5 V at an I_{bias} of 10mA.

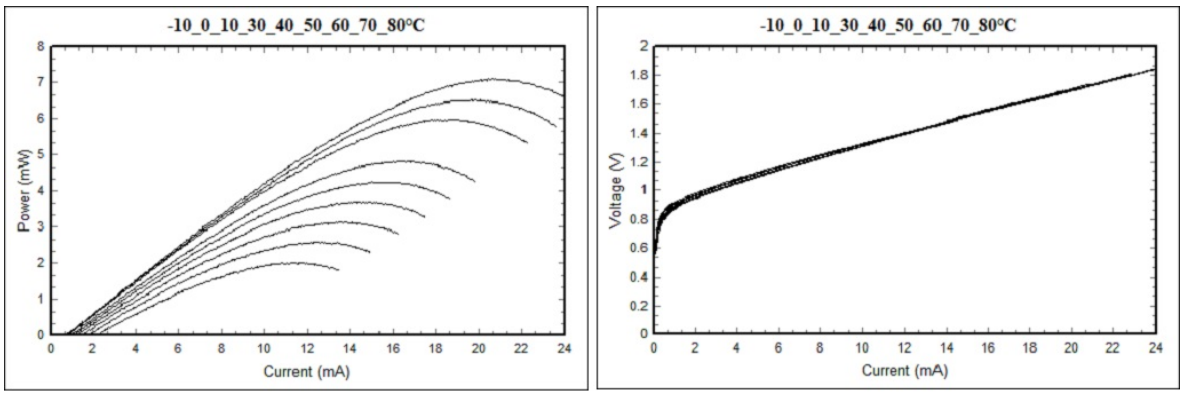


Figure 14. (Left) LI graphs from -10°C to 80°C; (Right) VI graph.

To provide several options for the optical coupling into the waveguides, VCSEL variants with 4 μm and 5 μm aperture have been designed and manufactured. For example, the FWHM of a 5 μm aperture VCSEL has been measured at ca. 14° and resulted in very good optical coupling with the waveguides. The VCSEL chip and contact layout enabled flip chip bonding that was successfully demonstrated by both VTT and TUE.

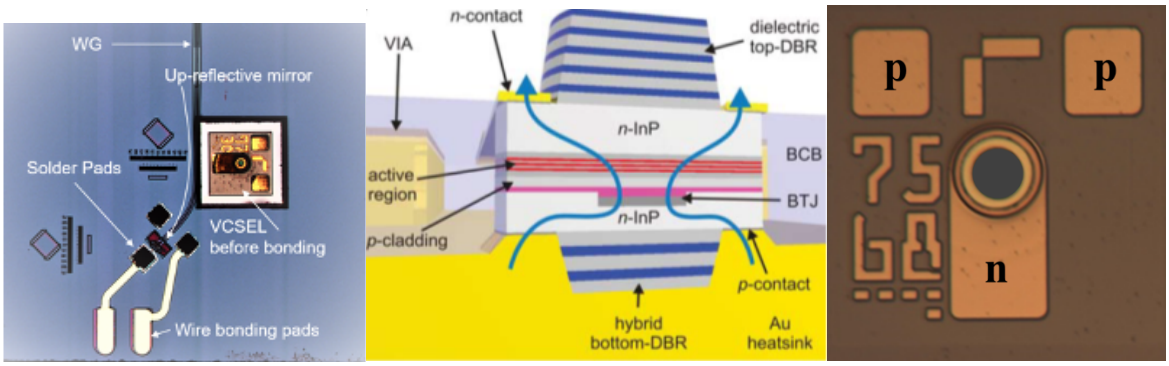


Figure 15. VCSEL top circular mirror (on the left), short cavity VCSEL structure (center) and chip layout (on the right).

3.2 VCSEL Alignment sensitivity during Flip-Chip Bonding from top

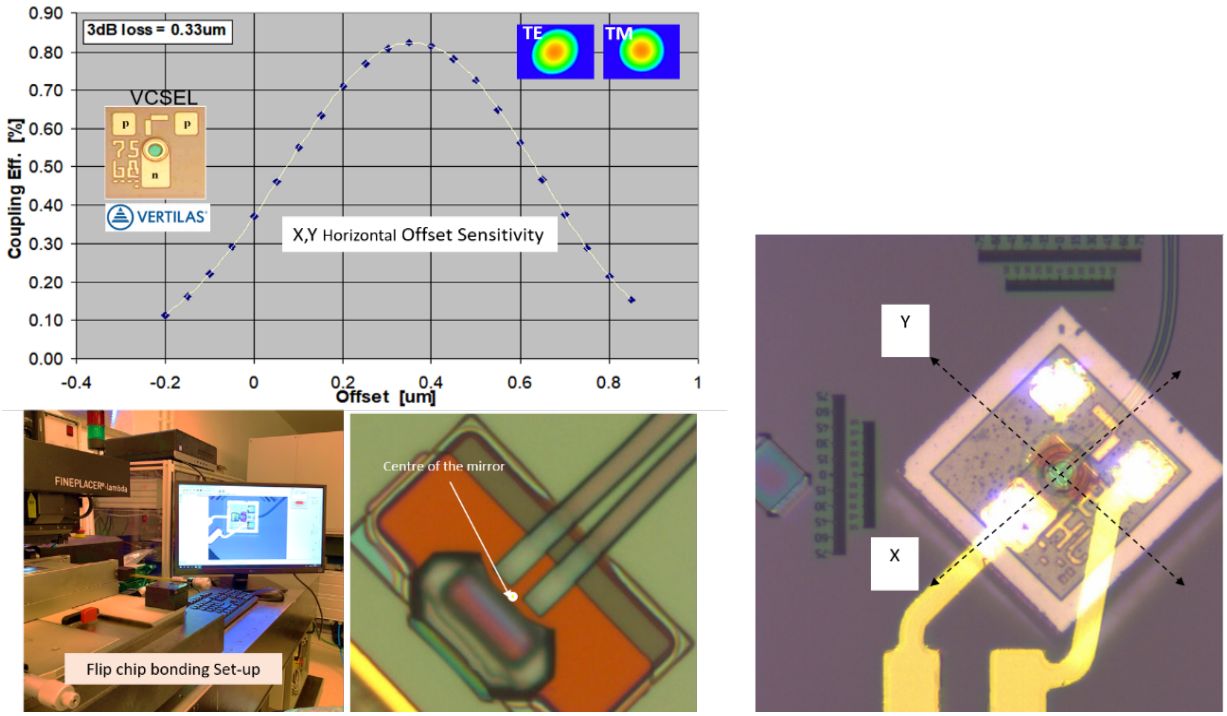


Figure 16 VCSEL alignment sensitivity during Flip-Chip bonding.

During FlipChip bonding process it was important to estimate the horizontal coupling sensitivity before to permanently bond any VCSEL in position. An important assumption was that the expected output beam profile from the VCSEL was circular (also for both TE-TM polarizations) so that horizontal alignment sensitivity was practically the same for X and Y bonding head direction as

shown in Figure 16. Expecting 3-dB VCSEL-MIRROR coupling losses with only 330nm offset part´s displacement, it appears evident how critical would be to have high placing resolution machine) coupling loss results after soldering.

3.3 ASSEMBLY USING BACK SIDE OF SIPH PIC

As an alternative, VCSELs are also considered to be co-integrated with down reflecting mirrors, which is developed by VTT as well. The VCSEL is embedded in the silicon substrate through backside process and flip-chip bonding. Electronic circuits are accordingly designed and fabricated on the backside, and the emitted light is coupled with the down reflecting mirror through the BOX layer. This approach has been intensively investigated to accomplish a dense (DWDM) transmitter MOD. In section 3.3.1 the details of the processing and initial test results for a DWDM VCSEL on SiPh based module are detailed. In section 3.3.2 we highlight extended work on solving the issues observed in alignment and coupling of VCSEL to 3μm silicon waveguide by co-integrating photo resist lanes on the PIC.

3.3.1 DWDM VCSEL and SiPh assembled transmitter concept (with backside coupling)

The Tx architecture developed in the PASSION project is aiming to support the use of directly modulated C-band VCSELs, multiplexed together using a SiPh PIC to create a 40 channel, 2 Tb/s single Tx MOD. In the effort to demonstrate this functionality, we have designed, fabricated and assembled a 4 channel transmitter. Unlike the approach followed by VTT, TUE made use of wet etching of the silicon substrate to allow the assembly of the VCSEL and IDT drivers on the bottom of the PIC. This has the advantage of shortening the transmission lines between the driver and the VCSEL with a potential gain in terms of signal integrity [1]. A schematic drawing of the assembly strategy is shown in Figure 17.

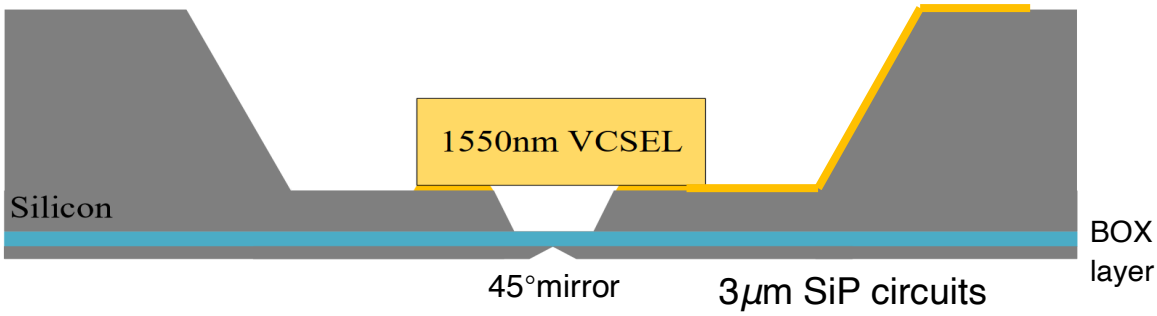


Figure 17. VCSEL assembly concept by embedding in cavity in back side of PIC.

In order to allow for compression bonding at the bottom of the recess created for the embedding of the VCSEL, the wet etching of the silicon wafer is halted when a 25-micron thick layer of silicon is still remaining. This will result in increasing coupling losses as will be shown below. For solving this problem please look at Section 3.2.2 where a system based on lenses is suggested.

The PIC provided by VTT is further processed in the TUE cleanroom with the required metalization layers for the flip chip assembly of VCSEL and VCSEL drivers on the back side and optical vias to allow light coupling. Figure 18 shows several SEM images of the processed silicon PIC.

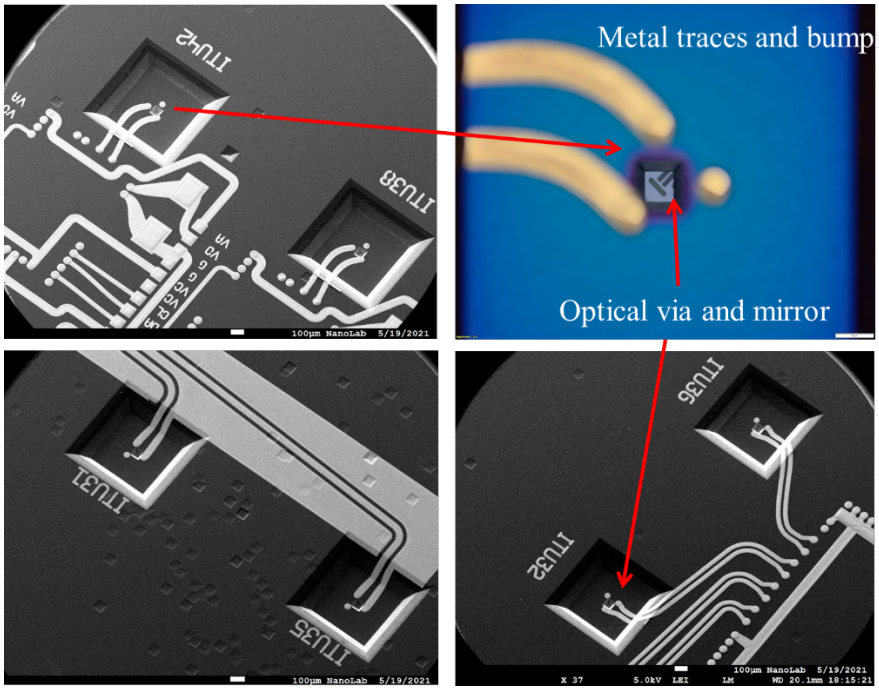


Figure 18. Optical and SEM images of processed back side of PIC.

In order to test the optical coupling of light via the downward reflecting total internal reflection (TIR) mirrors, lensed fibres were used for light injection and collection. The entire optical circuitry is included in these measurements (TIR mirrors at input and output, the AWG and the two Mach-Zehnder Interferometer - MZI - interleavers). In Figure 19 the measured optical output power after the multiplexing and interleaving stage is given, for light injected through several different inputs labelled by the ITU channel number representing them.

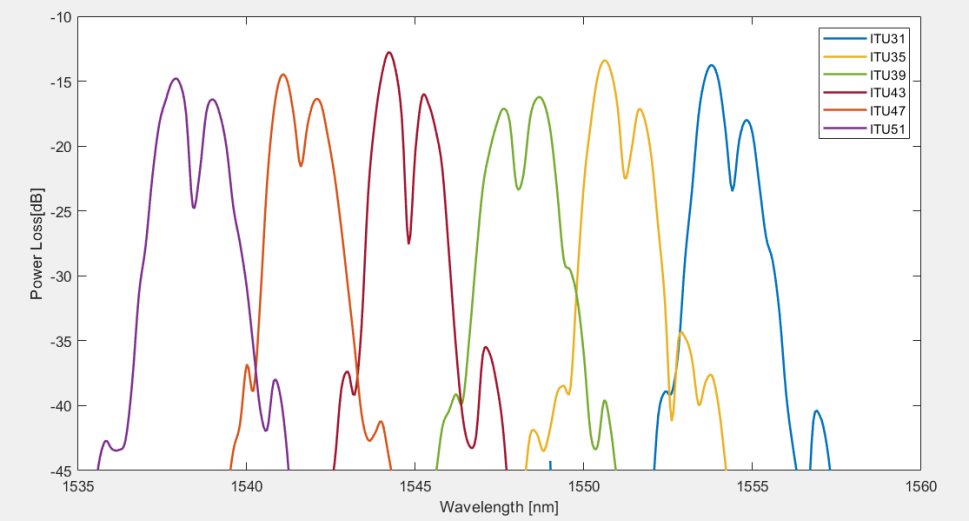


Figure 19. Measured optical losses for light injected via a lensed fiber into a channel input and measured at the multiplexed output.

It is visible, that the different channels have roughly the same channel width imposed by the AWG design and that the expected smooth transfer function is superimposed with the interleaver response. The average loss per channel, based on the use of lensed fibre input and output coupling is ~15dB. To complete the assembly of the DWDM transmitter module, 4 VCSELs with a 400GHz

wavelength spacing were selected and flip-chip bonded into the cavities on the SiPh PIC. Figure 20 shows the back side of the PIC with embedded VCSELs and the spectrum of the 4 VCSELs as they are multiplexed through the AWG and interleavers in the PIC. Due to possible misalignment in VCSEL positioning, the increased distance between VCSEL aperture and TIR mirror (required to ensure sufficient rigidness under compression bonding) and limited access of output lensed fibre, the coupling losses where on average >35dB. This was inhibitive for the measurement of modulated signal as signal to noise ratio (SNR) was insufficient to capture the resulting data signals. A possible solution to this problem is sketched in Section 3.3.2 where the improved coupling using a photoresist lens is detailed.

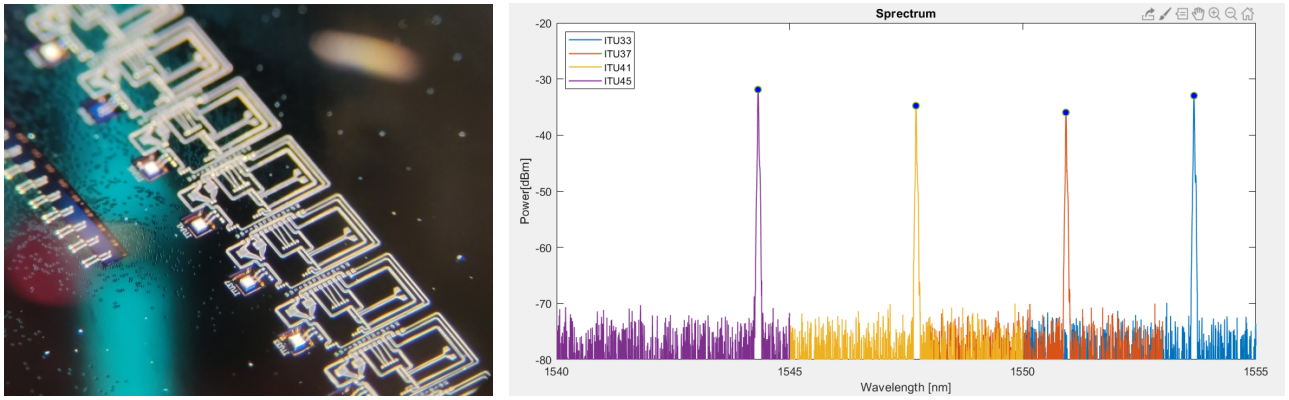


Figure 20. Image of back side of SiPh PIC with embedded VCSELs (Left); Spectrum of 4 VCSELs as captured at the output of the SiPh PIC multiplexer (Right).

3.3.2 Improving VCSEL to SiPh light coupling using on chip lenses

In order to further enhance the coupling of light into the silicon waveguide, also an alternative solution based on the co-integration of a photoresist (PR) lens in the optical path has been explored. The package scheme is proposed and shown in Figure 21.

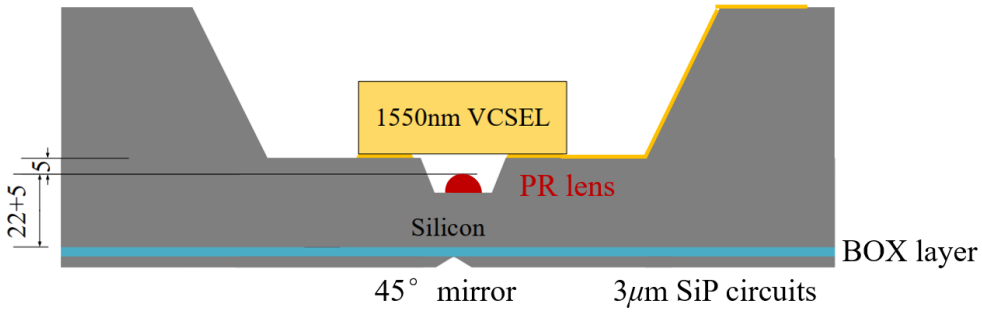


Figure 21. Integration scheme of VCSELs and down reflecting mirrors including PR lens.

There are several advantages of this integration scheme. Firstly, the down reflecting mirror is easier to fabricate. Secondly, the electronic circuits and photonic circuits are separately designed on both sides of the wafer. Thirdly, the shorter distance between BiCMOS driver and VCSEL can be realized to ensure the sufficient RF performance. Finally, in order to overcome the expected additional coupling losses when compared to flip-chip assembly above the Silicon waveguide, photrefractive (PR) lenses have been developed and co-integrated in this new scheme.

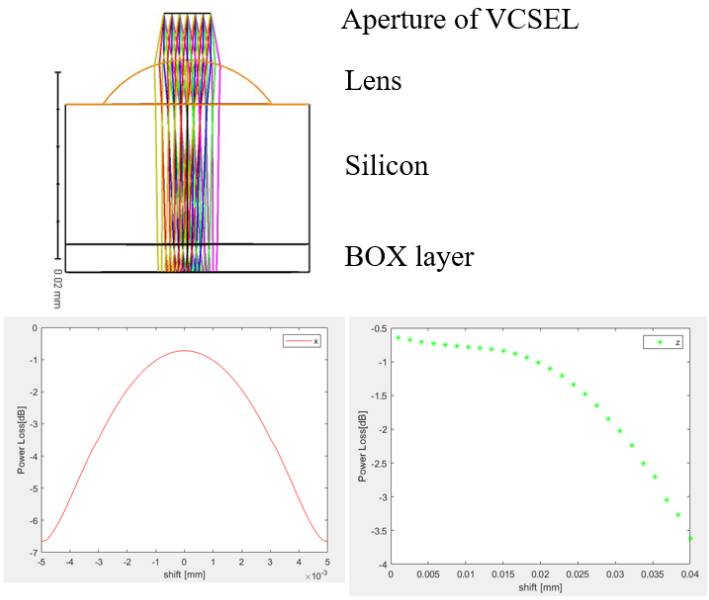


Figure 22. Zemax simulation results for lightcoupling between VCSEL and Silicon waveguide with the help of a PR lens.

To evaluate the concept expected performance, the PR lens is simulated (using the refractive index of the photoresist used) and the optimal object distance and image distance are numerically found by establishing the required cavity depth. The optical coupling system is designed in Zemax OpticStudio. The complete model and results of the simulation are shown in Figure 22. The output beam from the VCSEL is focused by a spherical photoresist lens, with the radius of curvature of 7.5 μm. In this packaging scheme, the best coupling loss is 0.7dB. We also simulate the placement tolerances, showing 3dB coupling loss of 5µm in x- and y-direction and 30 μm in z-direction.

The fabrication starts on a 6-inch SOI wafer. The waveguides are firstly fabricated, then TIR mirrors are formed at the end of waveguides by wet etching technology. As the fabrication results show in Figure 23, a smooth mirror is formed thanks to the etching along a silicon crystal plane.

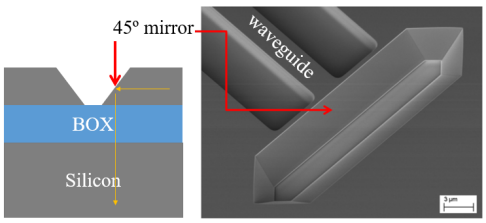


Figure 23. schematic drawing (left) and SEM photo of waveguide and TIR mirror. The yellow arrow indicates the light path.

Then, the patterned wafer (with the SiPh circuitry) is diced into 40mm x 40mm samples for testing the process on the bottom side of the wafer. The cavities for VCSELs and lens embedding are patterned and formed by wet etching of the silicon substrate. Then, the lens is patterned by double-side lithography to achieve the best alignment accuracy. After photoresist reflow, the electronic circuits and bumps are patterned by plating. The process results are shown in the SEM photos with the plating seed layer, in Figure 24.

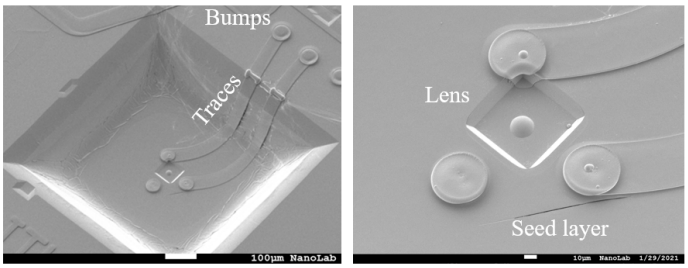


Figure 24. SEM photos before removing the plating seed layer: fabricated cavities for the single VCSEL (left). Zoom-in photo of small cavity and lens and pads for VCSELs (Right).

Three-dimensional mapping of the small cavity and microlens is obtained with a profilometer. In Figure 25 we see that the small cavity is 11.9 µm deep and that the height of the micro lens is measured to be 4.5 µm in both the x- and y- direction.

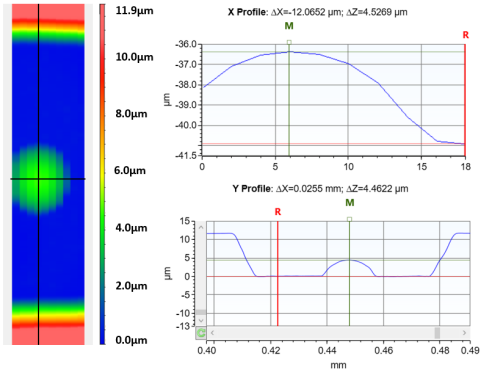


Figure 25. Measured 3D map for the lens in the small cavity, both x- and y- profile indicate the height of the micro lens is 4.5µm and radius of curvature is 10.9µm.

To characterize the photonic circuit design, the 45° mirrors are fabricated at both input and output of a straight 3 µm waveguide. Two lensed fibres, with a 2 µm mode field diameter, are placed vertically on top of the mirrors. However, because of the thin layer of silicon (kept in place to ensure the correct imaging distance between VCSEL and mirror, the fibre can not be placed at the optimal distance from the TIR mirror leading to high coupling loss, shown in Figure 26.

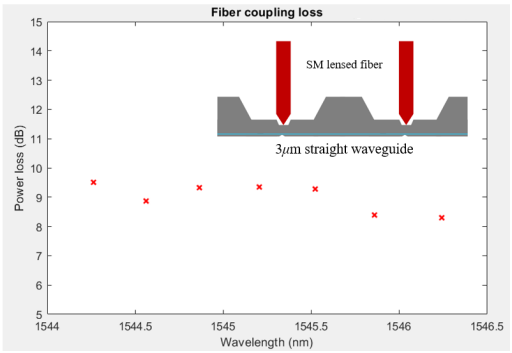


Figure 26. calibration measurement in the VCSEL tuning range by using two lensed fibers. Insert: test scheme shows two vertically aligned lensed fibers and mirror on both sides of the straight waveguide.

The coupling loss is wavelength-dependent, and the lowest coupling loss of fibre to mirror is measured to be 8.2 dB. Here, we assume there's no loss on the 3mm long waveguide. In future

designs, the input and output need to be patterned separately, and the silicon layer at the output will be removed, or a lens will be designed for the fibre alignment.

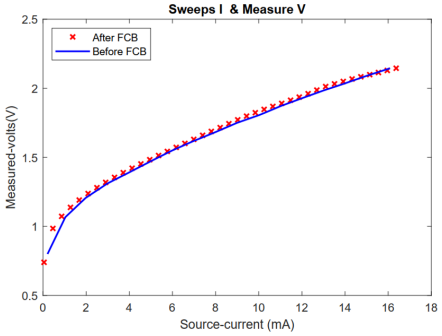


Figure 27. IV curve of the VCSEL before and after bonding.

After characterizing the straight waveguides and mirrors, the single-mode VCSEL is flip-chip bonded with passive aligning between aperture and lens. The current-voltage curves of the VCSEL are compared in Figure 27, before and after the flip-chip bonding. This indicates the VCSEL is well connected with the circuits.

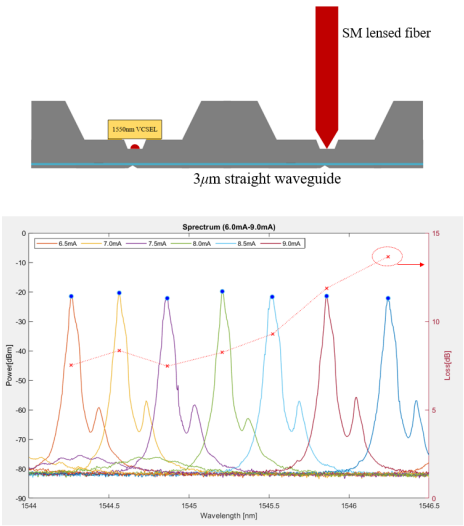


Figure 28. Spectrum measurement after VCSEL bonding. The calculated power loss of the lens system.

Finally, the coupling performance is tested. Firstly, the spectrum of the VCSEL is measured with changing current to identify the laser wavelength. As shown in Figure 28, from 6 mA to 9 mA, the wavelength shifts from 1544.26nm to 1546.24nm, and power increases from 1dBm to 3.3dBm. By deducting the fibre loss, the calculated lens system loss is shown in Figure 28. The lowest coupling loss is 7.5dB. There are two reasons for the extra losses. Firstly, the fabricated lens has a larger radius compared with the design, which is due to the large gap between mask and photoresist in the lithography step. A defocusing compensation needs to be considered in the next design. Secondly, it is difficult to achieve sub-micron accuracy alignment in the high temperature bonding process. Low temperature bonding or local heating techniques will be employed in the future.

4 EXPERIMENTAL TESTING OF THE FULL TX MOD TECHNOLOGIES

In order to demonstrate the PASSION transmission technology at the base of the PASSION S-BVT and incorporated in the PIC full Tx MOD, multicarrier modulation, specifically DMT, was applied to a single channel, i.e. to the VERT VCSEL bonded to the IDT HXT-14100 driver. The performance was experimentally evaluated in terms of transmission capacity thanks to the exploitation of the off-line adaptive digital signal processing (DSP). Multi-channel transmission was also evaluated thanks to the simulation tool developed to model VERT VCSEL direct modulation performance taking into account chirp associated to the experimentally measured linewidth-enhancement factor α and laser-specific adiabatic constant κ ($\alpha = 3.7$ and $\kappa = 1.526 \cdot 10^{13}$ Hz/W) [2].

4.1 SINGLE CHANNEL HIGH SPEED MODULATION RESULTS

The evaluation of the system performance is performed in terms of transmitted capacity in function of the system optical signal to noise ratio (OSNR). The employed experimental setup is shown in Figure 29. The tested C-band VERT VCSEL emits at 1535.2-nm, its measured linewidth is about 5 MHz and its equivalent electrical modulation frequency response is about 15 GHz, which considers both the intrinsic modulation properties and the extrinsic device parasitic components. The VCSEL is bonded to an IDT HXT-14100 driver which uses an I²C interface to provide both the bias and the modulation currents (as described in D3.2). Various combinations of bias and modulation currents have been tested; finally, the couple of values limiting the frequency chirp insurgence and reducing the penalty due to single sideband (SSB) filtering has been chosen: the bias current is set at 9 mA, while the modulation depth is fixed at 8 mA. The driver is connected to a 100 GS/s MICRAM digital to analog converter (DAC 10002) with 40-GHz electrical bandwidth and 6-bit vertical resolution which generates the electrical DMT signal. The DAC is controlled by the off-line adaptive digital signal processor (DSP) which calculates by Matlab® the dual side band (DSB) DMT modulation signal. The signal is composed of 256 subcarriers in a 20-GHz range, so the subcarrier spacing is 78.125 MHz. Moreover, to mitigate inter-symbol interference, a cyclic prefix (CP) of 2.1% of the symbol length is added. The obtained electrical spectrum is shown in Figure 31 a). As the PASSION super-module includes operation at 25 GHz channel spacing, obtained with wavelength selective switches (WSSes), we tested also the performance of SSB DMT, which is optically performed with an optical processor, namely a Finisar Waveshaper (WS4000s) emulating the transfer function of a 25-GHz spacing WSS. The measured optical spectra of the DSB DMT signal, of the SSB optical spectrum and of the WSS emulated by the Waveshaper are shown in Figure 32 a), b) and c) respectively. Before detection in order to vary the received OSNR an erbium-doped fiber amplifier (EDFA) is employed as ASE noise adder, The transmitter output signal is received by a 14-GHz PIN photodiode keeping the received power to a fixed value of -1 dBm; it is worth nothing, in fact, that in absence of propagation the DMT signal is optimally received also with direct detection.

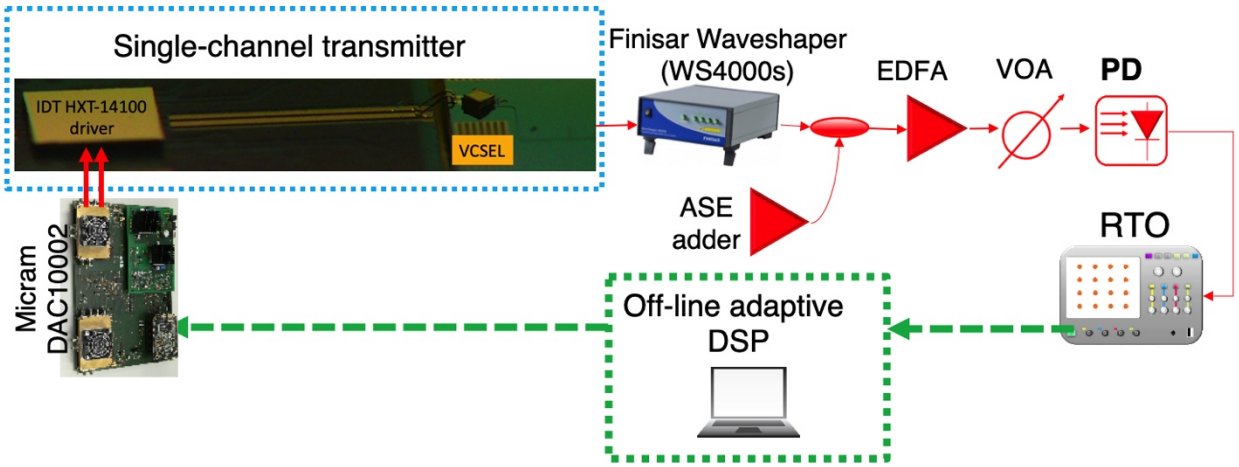


Figure 29. Experimental measurements setup.

The received signal is then acquired by a Tektronix real-time oscilloscope (RTO) with 8-bit vertical resolution, 100 GS/s and 33-GHz electrical bandwidth. Finally, the off-line adaptive DSP provides digital symbol synchronization, CP removal, sub-carriers phase recovery and demodulation, and bit error rate (BER) count. Optimal bit- and power-loadings (BL/PL) using Chow's algorithm with a target BER of $3.8 \cdot 10^{-3}$ (in order to exploit an advanced hard-decision FEC code with 7% overhead) are applied to adaptively assign the appropriate bit order at each sub-carrier during the mapping procedure.

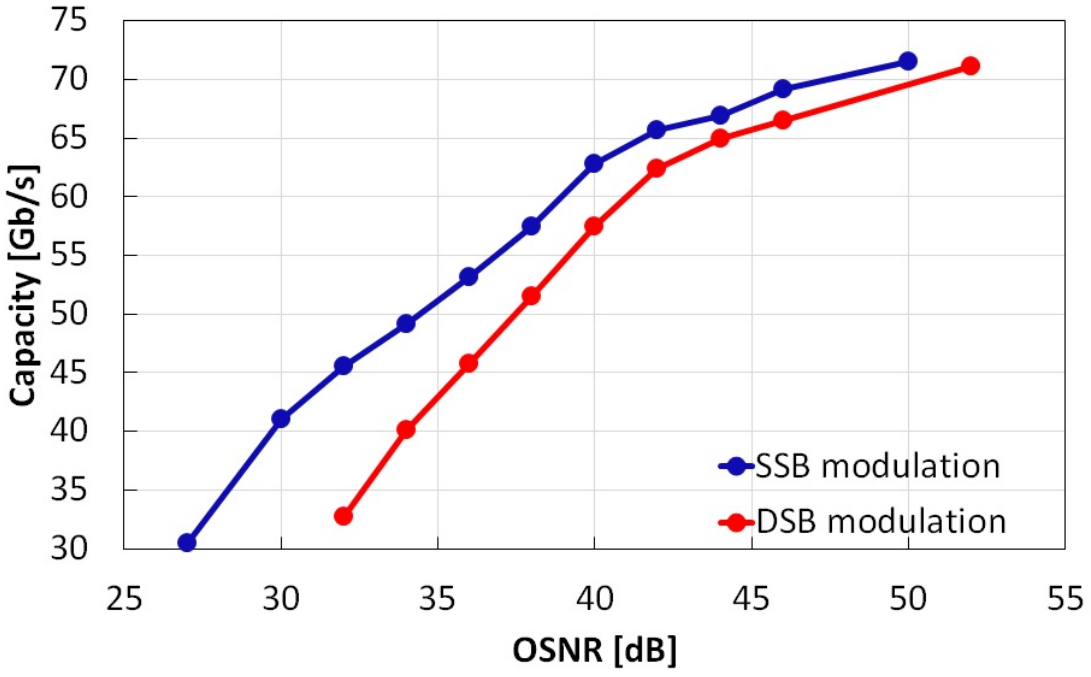


Figure 30. Measured capacities at the output of the single-channel transmitter for DSB and SSB modulations.

Figure 30 shows the capacities measured for SSB (blue curve) and DSB modulations (red curve) for OSNRs ranging between 28 dB and 52 dB. For both SSB and DSB modulations a capacity of more than 70 Gb/s can be achieved. SSB outperforms DSB modulation for all the measurement conditions, thanks to a better spectral efficiency and a better resilience to the introduction of noise due to power transfer between sub-bands during SSB filtering [2]. The power transfer, along with the

partial filtering of the carrier, reduces the carrier-to-signal power ratio (CSPR), defined as the ratio between the powers of the unmodulated carrier and the one of the modulated signal, of 1.5 dB for high OSNR conditions (16.9 dB in DSB modulation and 15.4 in SSB modulation). In turn the impact of spectral broadening due to the introduction of chirp, which affects the system performance, is limited for SSB modulation. Moreover, the increase of the signal power for SSB modulation leads to an increase of the transmitted capacity of 15 Gb/s with respect to DSB modulation in higher noise conditions (e.g., 32 dB of OSNR). The better resilience of SSB modulation causes a less tight requirement on the OSNR to achieve a given capacity with respect to DSB modulation: for example, 40 Gb/s can be reached at 30-dB OSNR for SSB modulation and for 34-dB OSNR when the optical signal is DSB-modulated. The target capacity of 50 Gb/s per channel can be achieved in DSB modulation for 38 dB OSNR and for 34 dB OSNR in SSB modulation.

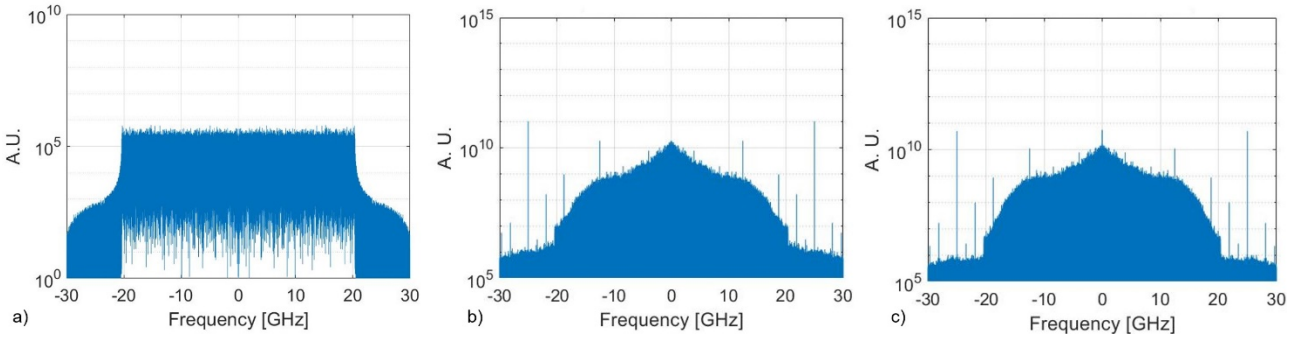


Figure 31 Electrical spectrum of a) DSB TX signal; b) RX signal of DSB-modulated VCSEL for 44 dB OSNR. c) RX signal of SSB-modulated VCSEL for 44 dB OSNR.

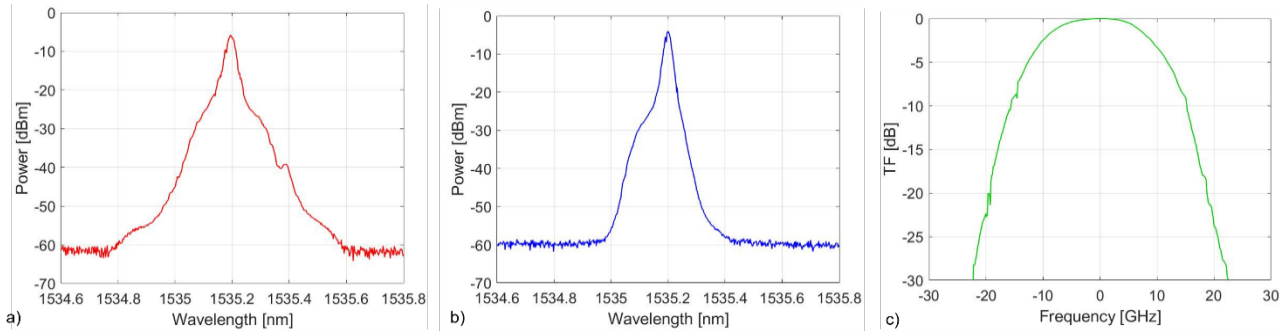


Figure 32 Optical spectrum of a) DSB-modulated VCSEL; b) SSB-modulated VCSEL for 44 dB OSNR. c) Transfer function of the 25-GHz WSS, as emulated by the Finisar Waveshaper.

Figure 32 shows the optical spectra of the DSB-modulated and the SSB-modulated VCSEL. Due to the effect of chirp, the carrier is broader than in presence of an externally-modulated source, but this effect is partially limited by the SSB filtering. Moreover, the suppression of the right-sideband causes the filtering of the second mode at 1535.4 nm. Figure 33 shows the corresponding received electrical spectra for DSB and SSB modulation. As previously stated, by comparing the electrical spectra, a slight increase of the signal power can be observed up to 18 GHz for SSB modulation with respect to DSB modulation. Moreover, for both the modulations, the spectrum broadening due to chirp is evident in the first 5 GHz. At last Figure 33 shows the comparison between the SNRs in DSB modulation (red curve) and SSB modulation (blue curve) for a) 44 dB OSNR and b) 32 dB OSNR. For 44 dB OSNR the DSB SNR is at most 2 dB higher with respect to SSB SNR in the first 7 GHz due to a slight subcarrier reduction due to SSB filtering, and then it is lower between 11 GHz and 16

GHz due to the signal power increase. Overall, SSB modulation gains 2 Gb/s more capacity with respect to DSB modulation at such high OSNR.

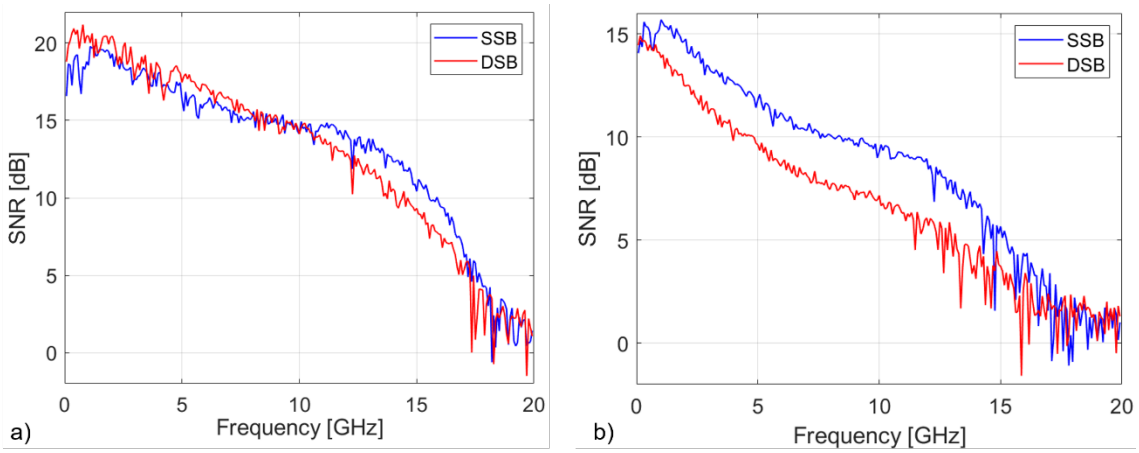


Figure 33. SNR profiles of SSB-modulated (blue curve) and DSB-modulated (red curve) VCSEL for: a) 44-dB OSNR; b) 32-dB OSNR.

For lower OSNR the interplay between optical noise and chirp causes the DMT signal to be more impaired by the presence of optical noise in DSB modulation, and so the corresponding SNR is at least 2 dB lower at all frequencies up to 15 GHz. This leads to the capacity reduction of 15 Gb/s previously discussed. By observing the SNR trends for both DSB and SSB modulations, the limited electro-optical bandwidth of the VCSEL source (15 GHz) causes a lowpass-like profile of the SNR per sub-carrier, leading the SNR to range from high values (20 dB at 44-dB OSNR) to very low ones (3 dB at the same OSNR). This limits the achievable capacity, since the high-frequency subcarriers can be at most loaded with low-order modulation formats.

4.2 MULTI-CHANNEL TRANSMITTER EVALUATION

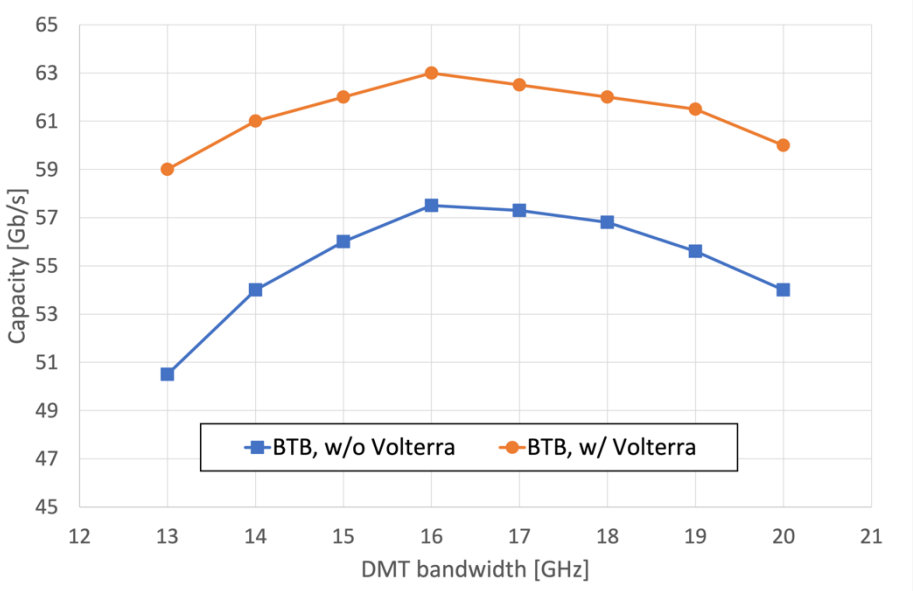


Figure 34. Multi-channel transmitter output capacities in function of DMT electrical bandwidth with (orange circles) and without (blue squares) Volterra equalization with 25-GHz channel spacing .

The performance in case multi-channel transmitter output was also evaluated thanks to the simulation tool developed to model VERT VCSEL direct modulation performance taking into account the laser chirp parameters, the bias and modulation current conditions and the electrical modulation frequency response. Directly modulated (DM) VCSELs are affected by a strong frequency chirp, which widens the channel optical spectrum. In the case of the PASSION super-module where the channel occupation is reduced to 25 GHz, this spectral broadening could be detrimental in terms of crosstalk among adjacent channels. The frequency chirp arising from direct modulation of VCSEL is composed of two components, one proportional to the emitted optical power (adiabatic chirp) and another related to its derivative (transient chirp); therefore, the electrical spectrum of the DMT modulating signal directly affects the frequency chirp of the VCSEL source and, definitely, the width of the resulting optical spectrum. We thus evaluated the PASSION transmitter performance in function of the DMT modulation bandwidth exploiting coherent detection with 45 GHz electrical bandwidth. In particular, the analysis has been carried out in case of multichannel transmission with 25 GHz spacing and SSB modulation obtained with the previously described WSS filter. Moreover, we also took in account the possibility to add to the off-line adaptive DSP a module providing equalization based on the Volterra algorithm (VE). The capacities at the output of the multi-channel transmitter for different DMT electrical bandwidths with and without VE are reported in Figure 34. It can be seen that for both equalization conditions the maximum capacity is obtained for around 16 GHz DMT modulation bandwidth, which represents a trade-off between the capacity increase due to the wider bandwidth and the decrease owing to the adjacent channels chirp-induced crosstalk. This optimal value is determined also by the VCSEL electro-optical bandwidth, which is 15 GHz. In this case, the VE allows a capacity improvement of approximately the 10%.

In conclusion, the technology adopted in the TX full module for the generation and transmission of the single channel has been validated. The employed VERT VCSEL with high bandwidth (15GHz) bonded with the selected IDT driver has demonstrated beyond 50 Gb/s rate thanks to DMT direct modulation. Also in case of aggregated capacity achieved by multichannel transmission, the exploitation of equalization techniques, such as Volterra equalization, allows to guarantee the target 2-Tb/s capacity per S-BVT module.

4.3 VCSEL OPERATION ON THE COMPLETE TX MOD

During assembly of the Tx MOD before sealing the upper lid (UL) an initial electrical test is carried out with the aim to check all VCSELs functionality together with the correct distribution of the power supply lines to VCSEL drivers. One of the major issues found during this phase was to probe the MOD outside its own EVB and fixation clamps. In fact, without the protection of the UL, the overall PIC, VCSELs, wirebonds and drivers are totally exposed to several undesired environments and possibly damaged by any physical contacts.

One way to simplify this initial test was to check VCSELs functionality (e.g. I_{BIAS}, $V_{FORWARD}$), leaving later the completion of electrical tests once the Tx MOD has been lidded, sealed and laid down on its EVB with clamps. For this test one specific low-count (4 ITU channels) MOD labelled MOD1-R3C5 has been used.

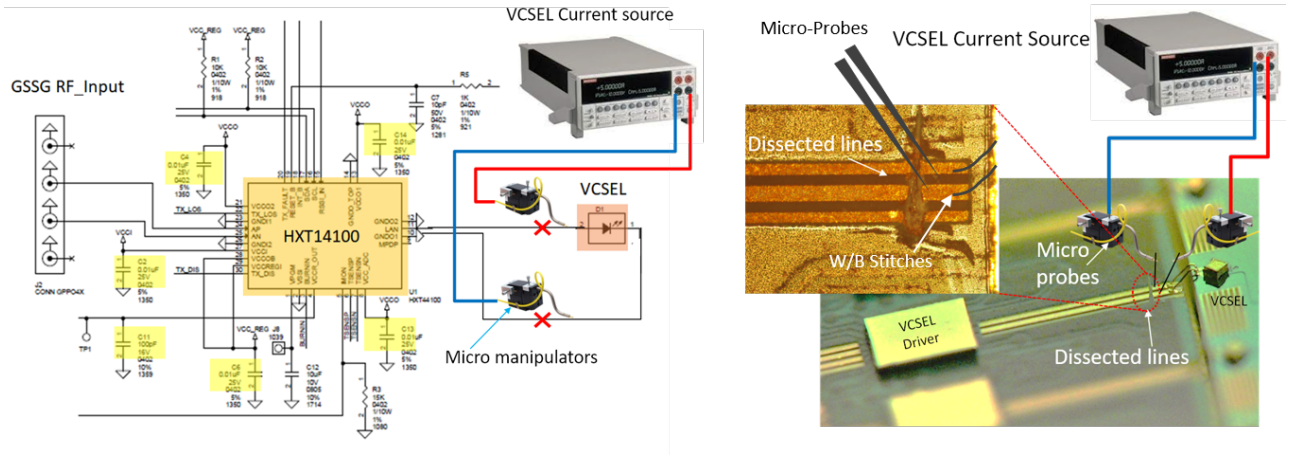


Figure 35 (Right) Probing VCSELs on the Tx MOD with external probes and precision current source . (Left) Insulating driver from VCSEL with dissected GSG lines, close to wirebonds.

We have dissected the GSG lines nearby the VCSEL wirebonding stitches (**Errore. L'origine riferimento non è stata trovata.**), to allow future possible re-works with slightly longer wirebond jumps (approx. 700μm). Then, probes and a current source were connected to remnant small pads toward the VCSEL wire bond stitches, (**Errore. L'origine riferimento non è stata trovata.** Left). By applying a current ramp I_{test} of 0÷15mA, we measured across the VCSEL the correct voltage value V_{FW} of approx 1.8V@15mA, while light scattering has been detected from an IR camera and reported in Figure 36. Figure 37 shows the Tx MOD output spectrum after the fibre pigtail, as can be seen at 12 mA of bias current the VCSEL correctly emits at the ITU channel 44; the overall IL accounting for all the PIC losses and VCSEL PIC coupling loss are of the order of 20 dB.

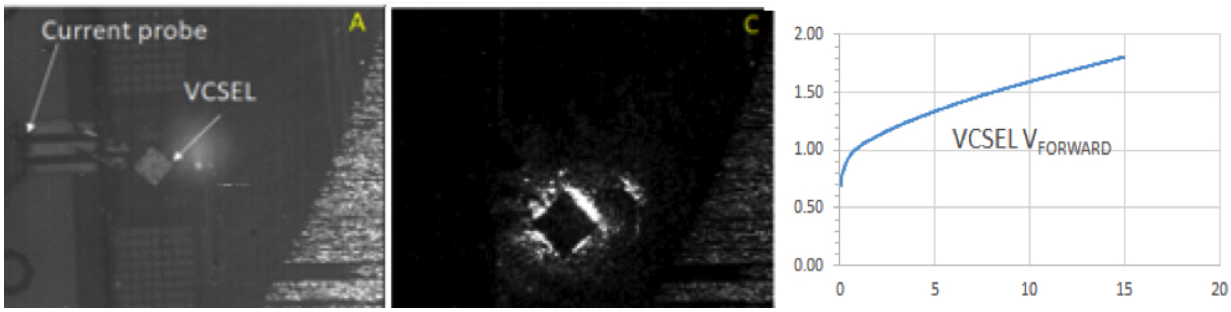


Figure 36 Probed VCSEL, IR light scattered, measured VCSEL voltage.

This test allowed to demonstrate the CW operation of the VCSELs flip chip-bonded onto the MOD PIC.

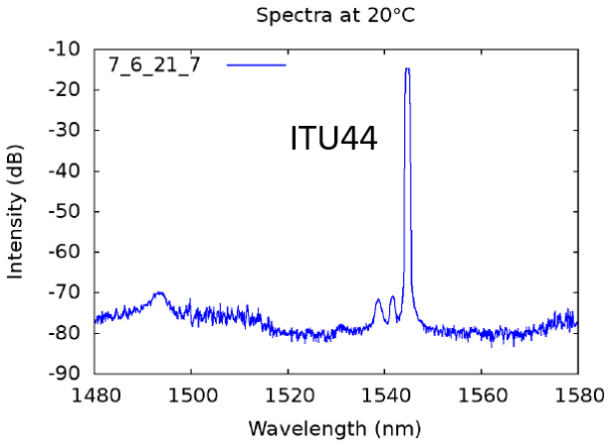


Figure 37 Tx MOD1-R3C5 output spectrum after the fibre pigtail at ITU channel 44.

4.4 FULL MODULE TESTING

After completion of the two Tx MODs counting a large number of channels, MPW9-R3C3 and R2C4, with 20 and 21 integrated VCSELs, respectively, unexpected and recursive reliability issues have not allowed to complete the testing of the functionalities of the fully assembled TX prototype. In fact, DC supply lines and I2C interface lines instabilities have been detected in the interconnection of the MODs to the EVB. All signals and power supply to the interposer are somehow blocked or limited in functionality nearby each single VCSEL driver, preventing any further possibility to connect and enable the drivers and succeed in performing the final tests. In particular, visual inspections and electrical tests performed on both modules inside the EVB show loss of I2C control interface and voltage supply distribution, measured only in proximity of VCSEL drivers. These evidences demonstrate a failure in the PCB interposer fabrication, not due to the technologies developed in the PASSION project. Further investigation is still in progress at the date of this report, with the metallographic analysis of a set of microsections. The interposer was fabricated by one of the most reliable manufacturers. Not only the PCB component was considered based on a mature and reliable technology, but also a special contract for a finger-probing lines continuity test was purchased. Despite this further caution the realized PCB interposer had serious malfunctioning. Although the failure of this component has not allowed the test of the full prototype, it did not compromise the validation of all the technological steps performed to realize the PASSION Tx MOD, nor the assessment of the Tx MOD functional operation.

5 CONCLUSIONS

The results presented in this document highlight the great progress obtained in maturing the PASSION Tx MOD concept into a viable product. All essential building blocks, including alternative assembly options, have been fabricated and tested with good results. The VCSEL and driver combination have proven to support single channel speeds way beyond the 50 Gb/s rate target and two fully assembled TX MODs were fabricated and housed in a specially made EVB.

Due to an unexpected issue with the manufacturing of the PCB which is part of the interconnection of SiPh PIC and the evaluation board, the testing of the fully assembled TX prototype was not completed. These issues are not due to the technology developed in the PASSION project but are related to a production failure of a mature component such as the PCB: hence, we confirm that the PASSION technologies adopted in the development of the Tx MOD have been effectively demonstrated.

6 REFERENCES

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[2] M. Rapisarda, et al., “Impact of chirp in high-capacity optical metro networks employing directly-modulated VCSELs,” in Photonics, vol. 5, no. 4. Multidisciplinary Digital Publishing Institute, 2018, p. 51

ACRONYMS

ASE amplified spontaneous emission
AWG arrayed waveguide grating
BER bit error rate
BL bit loading
CP cyclic prefix
CSPR carrier-to-signal power ratio
DAC digital to analog converter
DBR distributed Bragg reflector
DC direct current
DM directly modulated
DMT discrete multitone
DSB dual side band
DSP digital signal processor
DWDM dense wavelength division multiplexing
EDFA erbium-doped fiber amplifier
EVB evaluation board
FWHM full width half maximum
HW hardware
ITU International Telecommunication Union
LGA Land Grid Array
MFD Mode Field Diameter
MOD module
MUX multiplexer
MZI Mach-Zehnder Interferometer
OSNR optical signal to noise ratio
PCB printed circuit board
PIC Photonics Integrated Chip
PL power loading
PR phororefractive
RTO real-time oscilloscope
S-BVT sliceable bandwidth/ bit rate variable transceiver
SEM scanning electron microscopy
SiPh silicon photonics
SLD super luminescent diode
SMD surface mounted device
SMF single mode fiber
SMSR side mode suppression ratio
SNR signal to noise ratio
SOI Silicon-Over-Insulator
SSB single side band
SW software
TIR total internal reflection

TX transmitter
UL upper lid
VCSEL vertical cavity surface emitting laser
VE Volterra equalizer
WDM wavelength division multiplexing
WB wire bond
WSS wavelength selective switch