D3.6 Test results from the first transmitter submodule with directly modulated VCSELs

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EXECUTIVE SUMMARY

PASSION transmitter (Tx) module (MOD) based on 40 vertical cavity surface emitting lasers (VCSELs) and targeting up to 2-Tb/s capacity considers four 10-VCSEL sub-modules integrated together in the same silicon-photonics (SiPh) photonic integrated circuit (PIC), showing 10 VCSELS on each side. This report provides a detailed description of the fabrication and testing of the co-integration of VCSELs with the developed SiPh PIC, taking in account not only the 10-VCSEL s sub-module section, but the whole 40-VCSEL PIC. In fact, in the project development to maximize the Tx performance we directly moved to the design and realization of a single integrated 40-VCSEL PIC.

The re-design of the multiplexing block integrated in the Tx MOD PIC to combine the 40 VCSEL emissions in a single silicon waveguide is reported. Next to the main assembly approach which assumes top reflecting mirrors and hence VCSEL assembly on the top of the SiPh PIC, details regarding the thermal management design and radio frequency (RF) design based on a land grid array (LGA) interposer are shown with their characterization.

The description of the full Tx MOD development, including the evaluation board, and the demonstration of the technological solutions adopted for the full 40-VCSEL Tx MOD realization are presented in the deliverable D3.7.

1 INTRODUCTION

In the deliverable *D3.1 "Detailed design of the Tx module architecture and interfaces*" the details concerning the design considerations of the PASSION Tx MOD based on 40 VCSELs and targeting 2-Tb/s capacity were described. The adopted Tx MOD design considers four 10-VCSEL sub-modules integrated together in the same PIC (10 VCSELs put on each PIC size). This report will provide a detailed description of the fabrication and testing activities which were taken in order to check the co-integration between the VERT InP VCSELs and the VTT SiPh PIC, considering not only the 10-VCSEL sub-module section, but the whole 40-VCSEL MOD PIC. In fact, in the project development to maximize the Tx performance we directly moved to the design and realization of a single integrated 40-VCSEL PIC.

After a recap of the Tx MOD architecture and its modular structure adopted in PASSION, we describe the design, realization and characterization of the new 40-channel multiplexer (MUX) based on a single integrated arrayed waveguide grating (AWG), characterized by better performance with respect to the previous two stage MUX. The results of the assembly of coupled VCSELs to the SiPh PIC based on up-reflecting mirrors for 3D integration, together with suitable wafer-level tests are then reported. Finally, the thermal management design and RF design based on a LGA interposer for the final 40-VCSEL Tx MOD integration are shown with their characterization.

2 PASSION MODULAR APPROACH

One of the main objectives of the PASSION project is the development and deployment of a photonic sliceable-bandwidth-bitrate variable transceiver (S-BVT) to support agile metro networks, capable of enabling multi-Tb/s capacities per link. PASSION S-BVT is based on the realization of the innovative Tx MOD, exploiting 40 VCSEL sources, each one operating at a different 100-GHz spaced wavelength division multiplexed (WDM) wavelength over the C-band, directly modulated by the discrete multitone (DMT) format to obtain up to 50 Gb/s rate per VCSEL per polarization. Starting from this Tx MOD, aggregating a transmission capacity up to 2 Tb/s, a special fully-equipped Tx super-MOD enabling up to 8 Tb/s total capacity can be obtained. In particular, PASSION adopts a modular approach: just identical 40-VCSEL MODs are designed and developed. The 40 emitted wavelengths (spaced 100 GHz) from the VCSELs in each MOD can be properly tuned all together in a range of 0-75 GHz in order to achieve 4 different MODs with shifted channels. Combining 4 of such a MOD, thanks a suitable wavelength interleaver, the full 160-channels TX super-MOD is obtained, characterized by 25-GHz granularity and 8 Tb/s capacity, as shown in Figure 1. Thanks to polarization-division multiplexing (PDM), 16-Tb/s total capacity can be also achieved by combining the outputs of two Tx super-MODs orthogonal in polarization. Finally, exploiting spatial multiplexing, such as in case of a 7-core multicore fiber (MCF), more than 100 Tb/s aggregated capacity can be enabled per link (Figure 2).

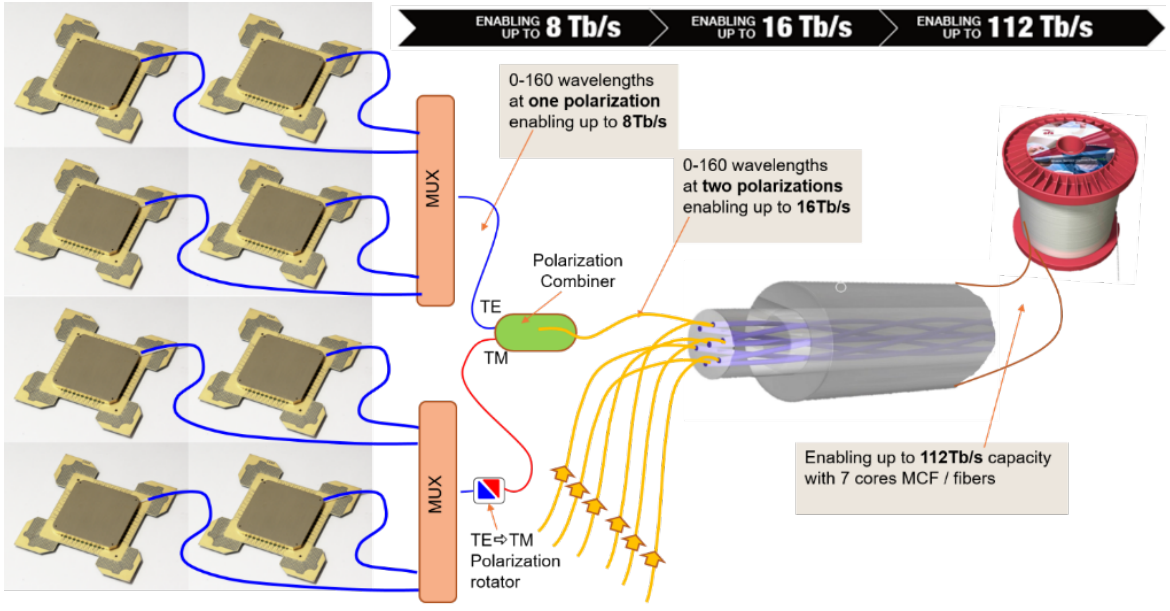

Figure 1. PASSION Tx modular approach for capacity aggregation exploiting spectral, polarization and space dimensions.

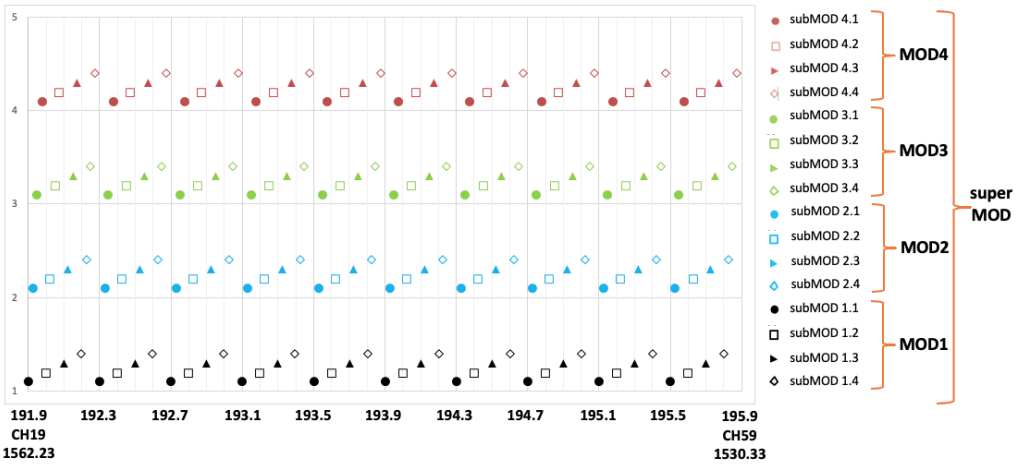

Figure 2. Grid of the VCSEL emission wavelengths for the 4 Tx MODs *constituting the* PASSION *super*-MOD.

3 PASSION Tx PIC WITH RE-DESIGN OF THE WDM MUX

In order to realize the Tx MOD targeting 2-Tb/s capacity thanks to the employment of 40 directly-modulated VCSELs, PASSION project was aimed to develop a new SiPh PIC with advanced functionalities, e.g. polarization-independent AWG necessary to combine a large number of channels (40 in PASSION Tx MOD), and improve the performance of existing components such as up/down reflecting mirrors and their hybrid integration with optically-coupled VCSEL lasers. One target of the technology development in PASSION was to optimize both short term and long-term production and R&D capabilities in VTT-Micronova on a wide scope, from the material and device development to electronics design and hybrid assemblies.

3.1 VTT SOI PLATFORM

For the challenging PASSION SiPh PIC, VTT has exploited thick silicon-on-insulator (SOI) waveguide technology, based on combining single mode (SM) rib and multimode (MM) strip waveguides, keeping light only in the fundamental mode to achieve effectively SM operation. VTT uses typically 3 μm thick SOI waveguides (Figure 3), where the light is strongly confined into the silicon waveguide core. Waveguide losses are small (0.1-0.15 dB/cm) for both rib and strip waveguides. Using large core waveguides brings significant advantages in the light guiding. Firstly, waveguide with large core can tolerate high propagating optical power in the waveguide (>1W). Secondly, the operating wavelength range is ultra-wide, reaching from 1.2 μm up to 6 μm. And finally, polarization dependency in the large size waveguide is small, for example, in square strip waveguides the birefringence can be even zero.

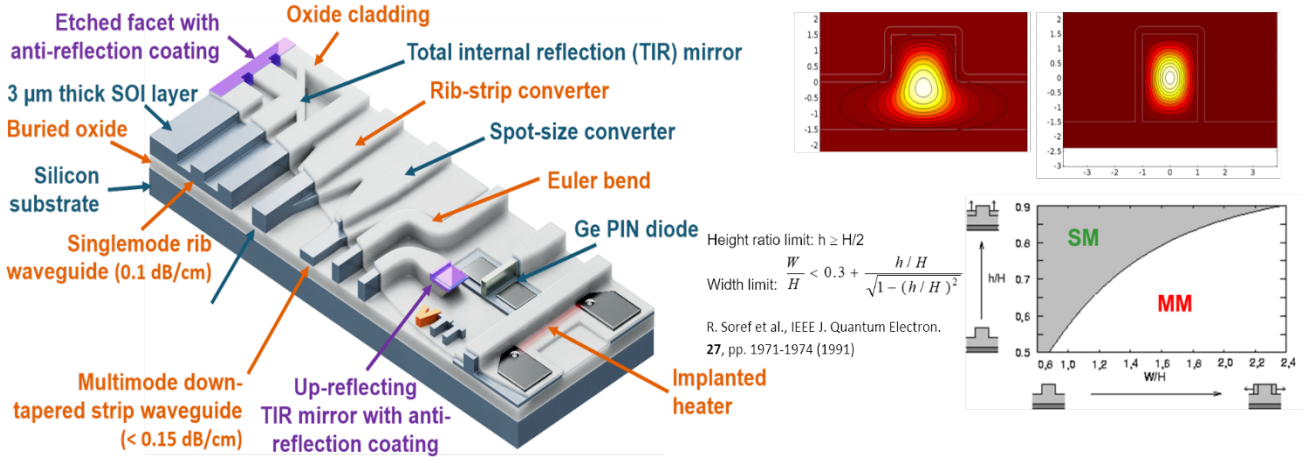

Figure 3. Schematic illustration of the 3 µm SOI platform with rib and strip waveguides, an adiabatic rib-strip converter, spot-size converter, horizontal and vertical total internal reflection (TIR) mirrors and compact Euler bends.

3.2 NEW 40-CHANNEL AWG DESIGN, FABRICATION AND CHARACTERIZATION

The Tx MOD architecture proposed in PASSION combines 40 ITU-T WDM channels from 19 to 58, with a spacing of 100 GHz. As discussed in Section 3 of the deliverable D3.3, there are many possible and competing designs about the 40-channel multiplexer (MUX), whether intended as a cascade of 5 MUXs (4 x 10Ch AWGs + 3 x Mach Zehnder Interferometers - MZIs) or more simply as a single MUX (1 x 40ch AWG). A preliminary solution of the Tx MOD PIC based on the multiplexing of the emissions of 10 VCSEL (spaced 400 GHz) put on each side of the PIC into a single output exploiting 1x10 AWGs together with a two-stage MZI for multiplexing the four 10-VCSEL sub-MOD outputs was successfully designed, fabricated, and characterized in transmission with TE polarization. A phase control mechanism (heater) on the longer arm of MZI to eventually tune-up the power to be delivered to the output port (for fibre-optic pigtailing) was also implemented. Measurement results have depicted good fidelity with the design targets. Alternative MUX elements combination for achieving the same interleaving functionality have also been investigated, particularly in collaboration with VLC. In fact AWGs and Echelle Gratings (EGs) have been embedded in separate wafer run and their characterization was provided. Satisfactory EG test results with insertion loss lower than 0.5 dB and cross-talk of -20 dB on the entire C-Band have been obtained. Channel interleaving has been achieved through a combination of various MUX elements, spanning a total channel-bandwidth of 4 THz (with the boundary conditions of 100 GHz channel-spacing and a total channel count of 40), as presented in Table 1.

Table 1 Possible MUX element interleaving combinations that can span 4 THz channel bandwidth with 40 channels spaced 100 GHz apart.

Stage I		
Channel Spacing (GHz)	**Input Channel Count**	**FSR (min.) (THz)**
100	40	4
400	10	4

With the aim to reach the best benefits in PASSION Tx MOD performance, we decided to move from the previous developed 4 x 10Ch AWG +3 MZIs structure to a more ambitious and challenging 1 x 40Ch AWG solution, realizing an additional SiPh PIC mask design. The added advantage is that the MUX design is completely passive, with consequent benefits in terms of power consumption with respect to the earlier design including interleavers and MZIs. The earlier MUX core is replaced with the new AWG design while everything else, such as VCSELs and contact pad positions stay in the original order and place to conform with the interposer design already in place as shown in Figure 4.

Due to some intrinsic characteristics of the VTT 3 μm SOI platform, a change of the MUX building block does not impact the architecture of remaining blocks embedded into the PIC, either from optical, electrical and even thermal point of views [1].

The new Tx MOD based on the 40Ch AWG design has been fabricated as part of the VTT MPW 9 process run. Initial test results (Figure 5) show that the 100 GHz channel-spaced 1x40 AWG design out-performs the previous design in terms of insertion loss (IL) (4.69-6.58 dB – Avg. 5.57 dB) and cross-talk (< -15 dB).

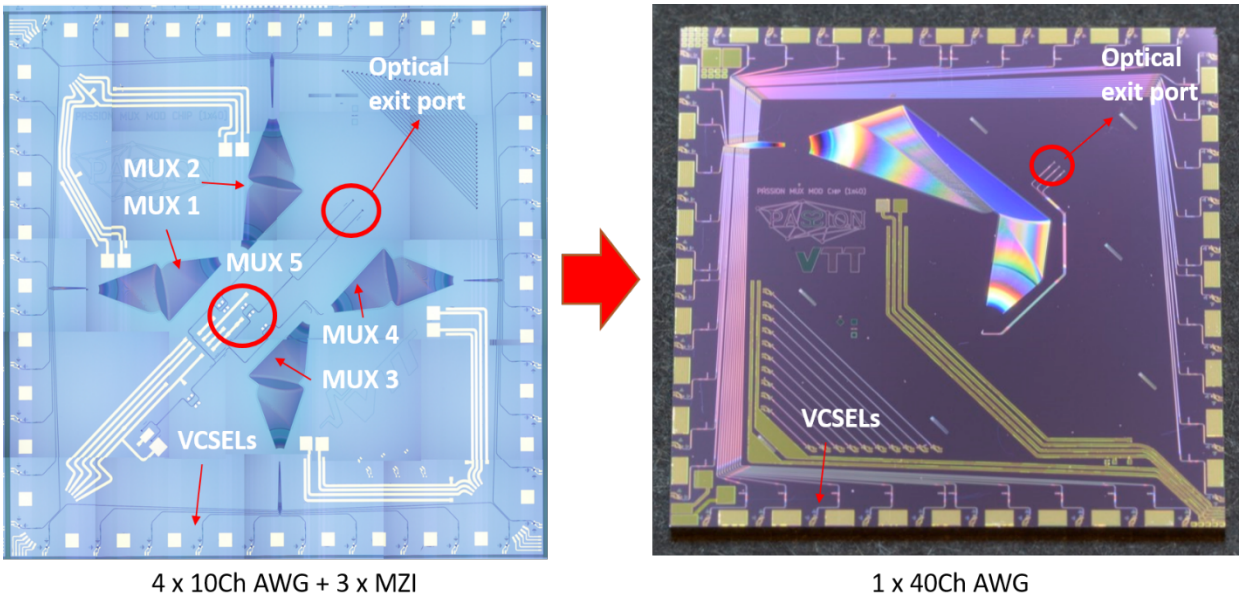

Figure 4 PIC design evolution to the new 40Ch AWG MUX.

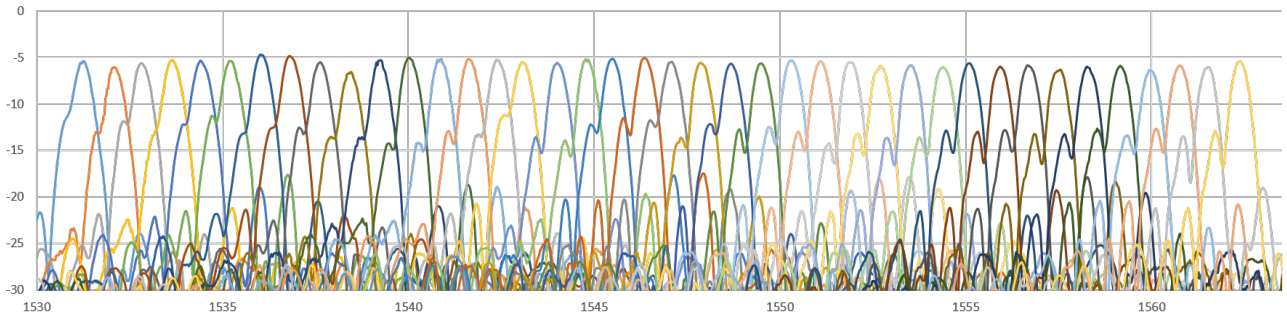

Figure 5 Characterization of 1x40, 100 GHz AWG.

Averagely, some slightly higher losses have been measured and traced back to cleanliness protocol failure for unexpected metal contamination and absorption into Si at the mirror facets in cleanroom. However, in several characterized chips, premium low IL values ranging from 3.5dB to 0.6 dB have been also reached (Figure 6).

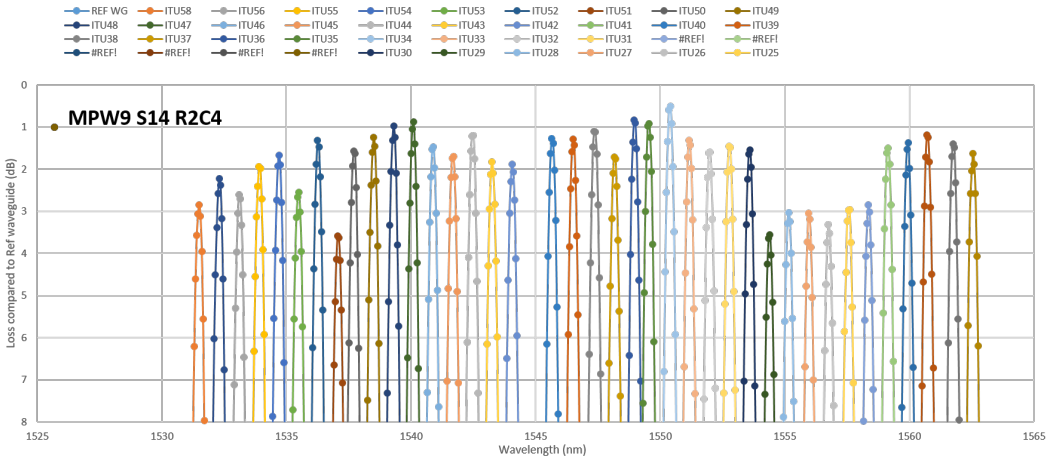

Figure 6 Low optical Insertion Loss obtained for 1 x 40Ch AWG.

Mechanical stresses in waveguide structures can cause anisotropic and inhomogeneous distribution of the refractive index and thus induce polarization dependency of the light guiding in an optical waveguide and therefore influencing the behaviour of the 1 x 40Ch AWG. For this reason, a COMSOL-based model for material stress profiles in SOI waveguide was developed. This model is an advancement of a previous model developed in OPEC project (Business Finland-funded): it allows to simulate waveguide birefringence taking in account real measured film parameters of the fabricated SOI waveguides. Birefringence modelling starts first by modelling a stress tensor for the fabricated waveguide structure based on material stress profiles (Figure 7 A and B). Next, coupling between refractive index tensor and the stress field is made (Figure 7 C). Finally, optical waveguide simulation can be made using layers with perfect match with the fabricated device (Figure 7 D).

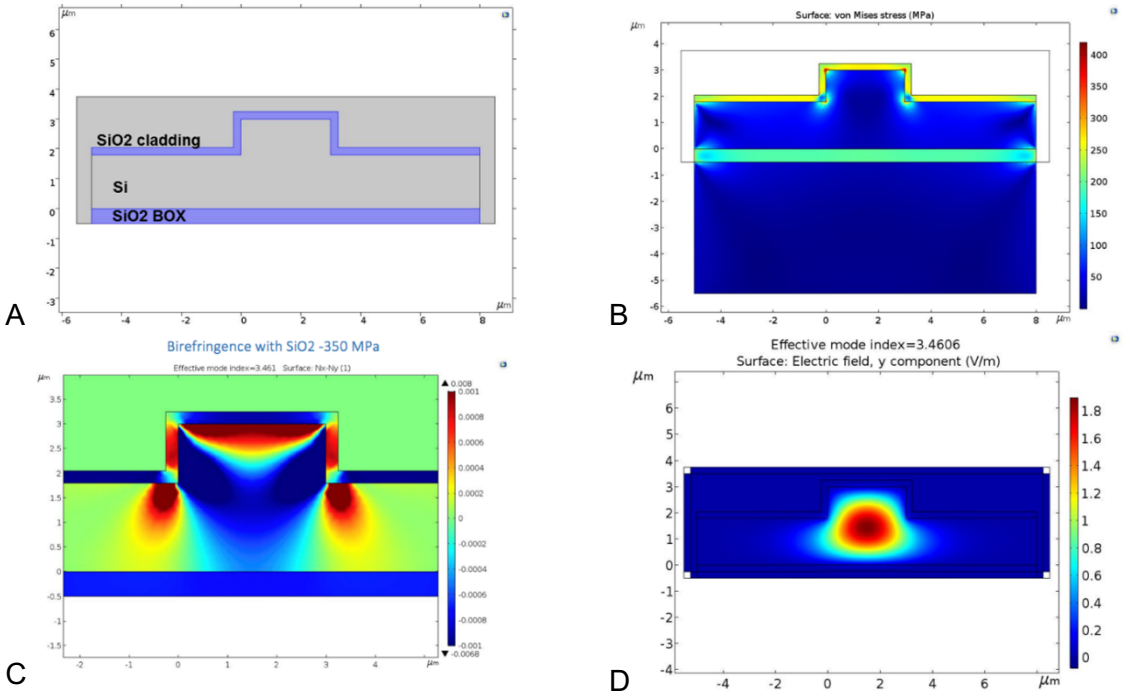

Figure 7. A: An example of a 3 µm rib SOI waveguide with 0.5 µm SiO2 buried oxide (BOX) layer and 250 nm SiO2 thermal oxide cladding. B: Simulated material stress profile with -350 MPa compressive stress in the oxide cladding (from literature) and -250 MPa compressive stress in the BOX. C: Modelled waveguide birefringence based on the stress profile in B. D: Simulated optical waveguide mode for TE.

Stress-optical measurements have been made during wafer fabrication processing and we used birefringence measurement results from fabricated SOI waveguides to create a model for evaluating intensity and location of stresses in structures with topography, such as those characterizing the AWG structure.

3.3 UP-REFLECTING MIRRORS FOR 3D INTEGRATION AND WAFER-LEVEL TESTING

Guiding optical signals in SOI chips is performed planarly, however the system integration would often require redirecting the in-out light perpendicular to the substrate. This is particularly relevant when VCSEL lasers and small profile fibre ports need to be coupled on SOI chip. One important advantage of the out of plane optical coupling is the possibility of wafer-level testing (WLT) of the fabricated SOI chips, greatly reducing the time to perform full electro optical (E/O) characterisation tasks. Also, the selection of best functional devices could then be done already before dicing the chips out of a wafer.

In thin SOI waveguides, the out of plane coupling is made with gratings. Grating couplers can be placed anywhere on the chip and they provide the possibility of WLT. However, they have limited bandwidth (~ 40 nm), and traditional designs usually have low coupling efficiencies (~ -4 dB) into the fibre. In PASSION, leveraging on 3μm SOI platform, up and down-reflecting mirrors have been designed and fabricated since of their very wide bandwidth (>300 nm) and low loss (<1 dB).

During SOI wafer processing, a wet etching process to form 45° tilted mirror planes in standard (100) silicon wafers has been used. To produce 45° tilted 110 mirror planes in (100) silicon the standard TMAH etching chemistry was changed acting on surfactant concentrations, process temperature and etching time. The resulted etched surface quality appeared satisfactory as shown in Figure 8.

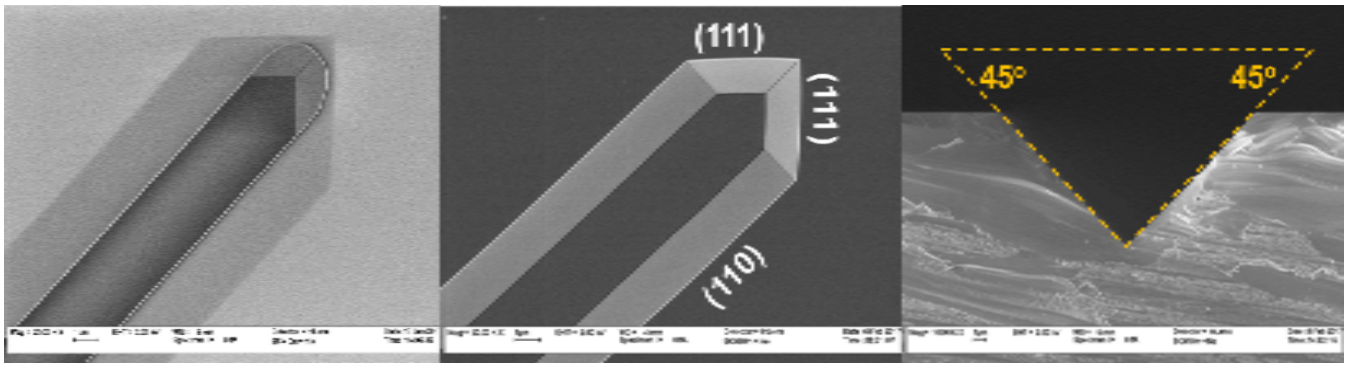

Figure 8 Wet etched mirror 45 degree tilted mirror planes (110) in silicon. Left: with oxide mask on. Middle: after removal of the oxide mask. Right: SEM image of the cross-section of a narrow etched groove with 45 degree tilted mirror planes.

In PASSION, only a total internal reflection (TIR) mirror has been fabricated, as it offers the highest possible reflection coefficient at any wavelength, and it is independent of fabrication tolerances. As shown in Figure 9, the mirror is clearly visible directly at the end of the waveguide.

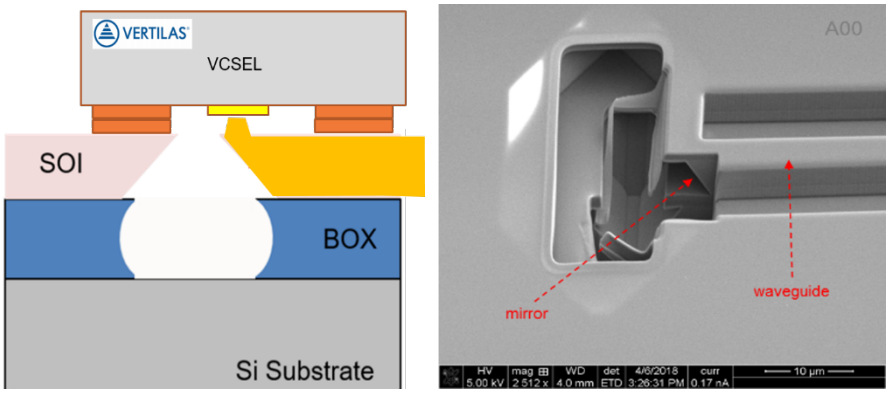

Figure 9 (Left) A schematic view of an internal up-reflecting mirror at the end of the 3µm waveguide. Light is totally internally reflected at the 45 degree tilted end facet of the waveguide. (Right) SEM image with TIR mirror plane exposed (using ion beam etching).

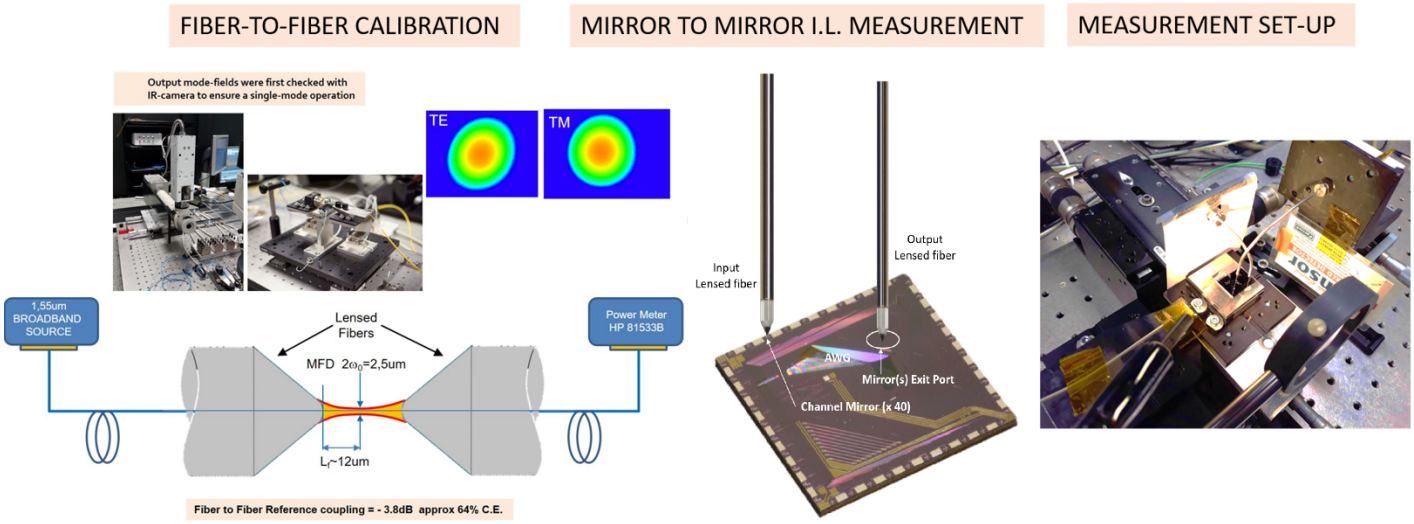

Figure 10 Up-reflecting mirror characterization setup.

A dedicated characterization setup for up-reflecting mirrors has been built up and shown in Figure 10. The setup simply consists of two tapered (lensed) PM fibers needed to respectively launch light from a broadband erbium doped fibre amplifier (EDFA) source into any channel mirrors of the PIC and collect light from one of the three exit-mirrors available at the AWG exit port toward an optical power meter.

Conveniently, the Si-PIC chip has also a set of available 10 straight waveguides for fiber-to-fiber and VCSEL-to-fiber calibration purposes (calibration structures). When used, the propagation losses within waveguides can be neglected (< 0.05 dB). Both mirror facets of calibration structures as well as all other existing mirrors on PIC have been anti-reflection (AR)-coated to reduce measurement

instabilities and coupling losses. A total coupling loss of averagely 5.5 dB has been measured, as shown in Figure 11.

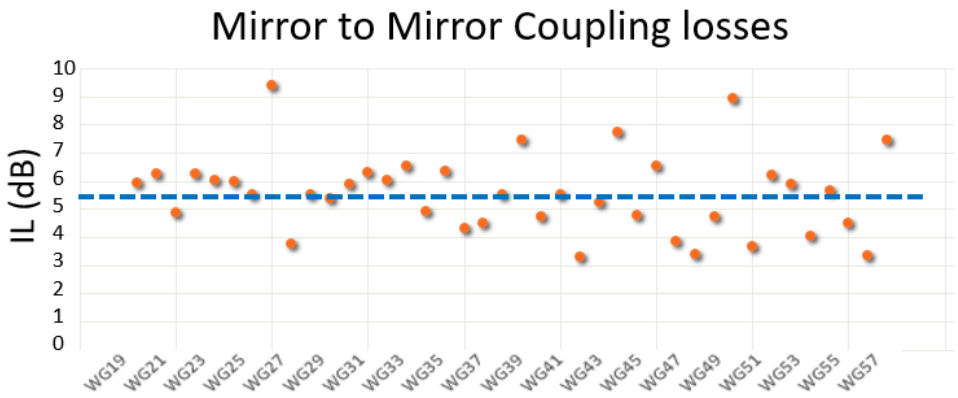

Figure 11 Plots for coupling loss analysis of the up-reflecting mirrors.

4 CO-INTEGRATION WITH VCSELS AND PIC CHARACTERIZATION

As described in the Introduction, with respect to the proposal where 10-VCSEL sub-MODs were considered, in PASSION final design the 40-VCSEL Tx MOD presents 10 VCSELs on each side, integrated in the same SiPh PIC, with their emissions multiplexed all together by using just a single integrated 1x40 AWG. Figure 12 shows the evolution of the Tx MOD from the original concept (first on the left) constituted by 4 10-VCSELs sub-MODS on each side, to the single AW-based PIC design, to the picture of its fabrication and finally on the right the Tx MOD integration with the electrical interposer.

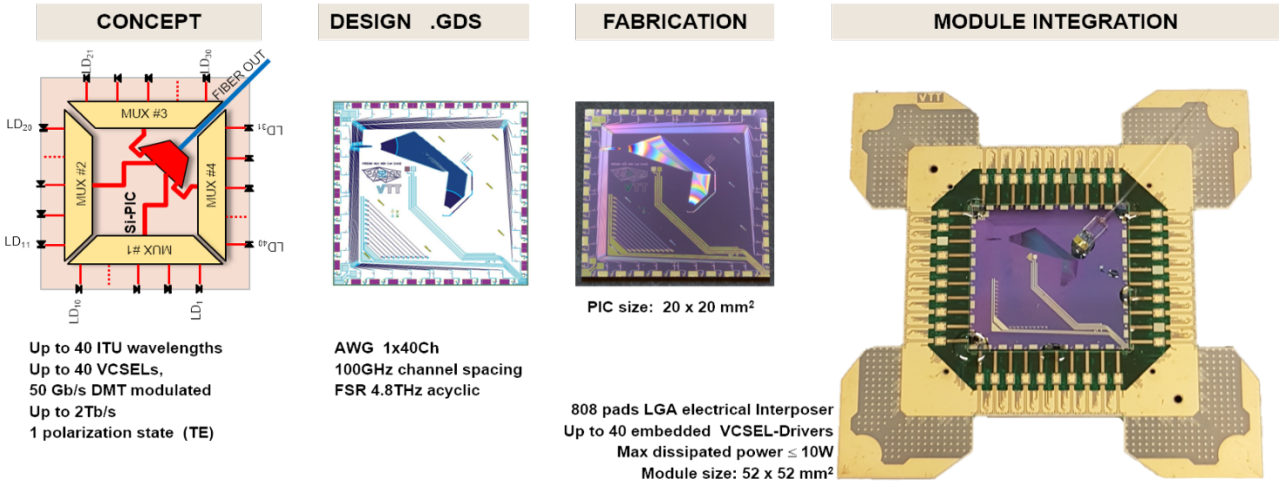

Figure 12. PIC from concept to fabrication and integration in the Tx MOD.

In the following we describe the selection of the VCSELS necessary for the realization of the Tx MOD and the integration issues, in terms of bonding, thermal and RF design.

4.1 VCSELS SELECTION

In PASSION project, the InP VCSEL sources are developed and produced by the partner VERT with the following targets:

- single-mode operation;
- low power consumption < 35mW
- output power about 4 mW @ 20°C
- bandwidth S_{21} = 20GHz
- layout optimized for flip chip bonding
- far field FWHM < 12°
- SMSR > 35dB
- low threshold current I_{th} < 2.5 mA @ 20°C.

For the realization of the PASSION Tx MOD, VCSEL emissions have been required to cover the whole frequency range from 191.9 THz (corresponding to the ITU-T WDM channel CH19 at 1562.23 nm) to 195.9 THz (CH59 at 1530.33 nm). Long-wavelength emission is usually critical owing to laser heating due to poor thermal conductivity and increased thickness of long-wavelength DBRs as well as the stronger temperature dependence of the threshold current. VERT approach overcomes these problems by employing a high-reflective and thermally well-conducting hybrid metallic/dielectric mirror together with a buried tunnel junction (BTJ) to enable low-resistance lateral current confinement and wave-guiding. The needed high modulation bandwidth (around 15 GHz) requires to adopt a short-cavity design (Figure 13). This has been achieved by means of a very short resonator length and an active region optimized for high bandwidth. Such a bandwidth allows to directly modulate the VCSEL in order to achieve up to 50-Gb/s signal rate per each VCSEL, by exploiting DMT or PAM modulation (e.g. 4-PAM modulation) [2].

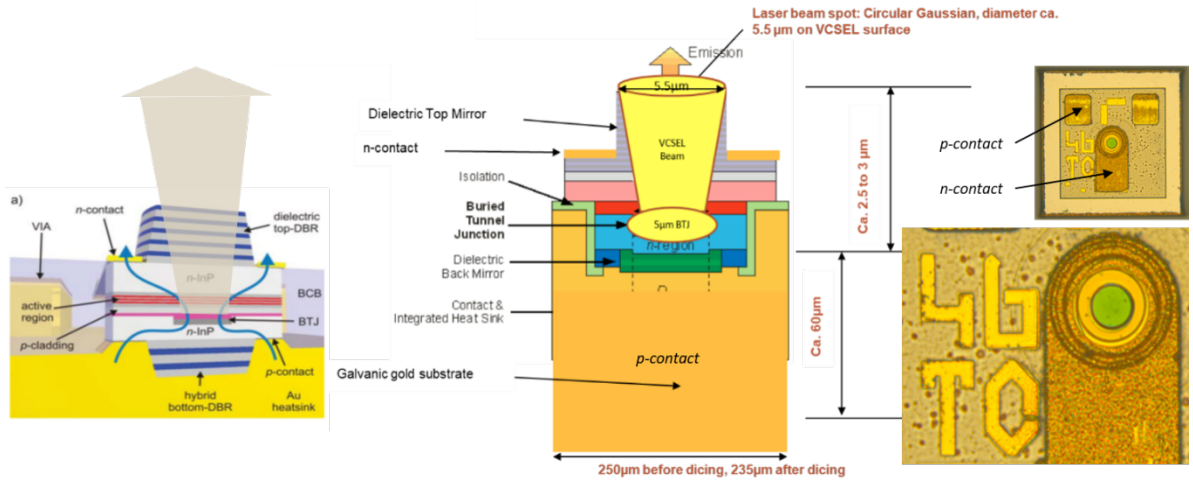

Figure 13 Cross section of the short-cavity VCSEL optimized for high modulation bandwidth.

Moreover, PASSION requires that 40 VCSELs are selected to match with the design of the WDM multiplexers in the Tx MOD with 100-GHz spacing. To satisfy this requirement the VCSELs have been designed and fabricated to target different emission wavelengths covering the C-band. Wavelength emission tuning of all the 40 VCSELs together in each Tx MOD in a range 0-75 GHz can be thermally achieved for the implementation of the 4 Tx MODs following the PASSION modular approach. Further tuning over the 25-GHz grid can be achieved through bias current tuning.

A wide wavelength tunability is obtained by changing the bias current, as demonstrated in Figure 15Figure 14 for two different devices A and B. The current tuning coefficient of the VERT VCSELs is ca. 0.3 nm/mA, which can vary accordingly to the applied current and the working temperature. Temperature tuning coefficient is reported to ca. 0.1 nm /°K. Moreover, Figure 14 shows the operation of the VERT VCSEL as a function of the bias current. To exploit the full S21 bandwidth, the I_{bias} should satisfy the relation $\sqrt{I_{bias} - I_{th}}$= 2.5/3 achieving the maximum modulation bandwidth.

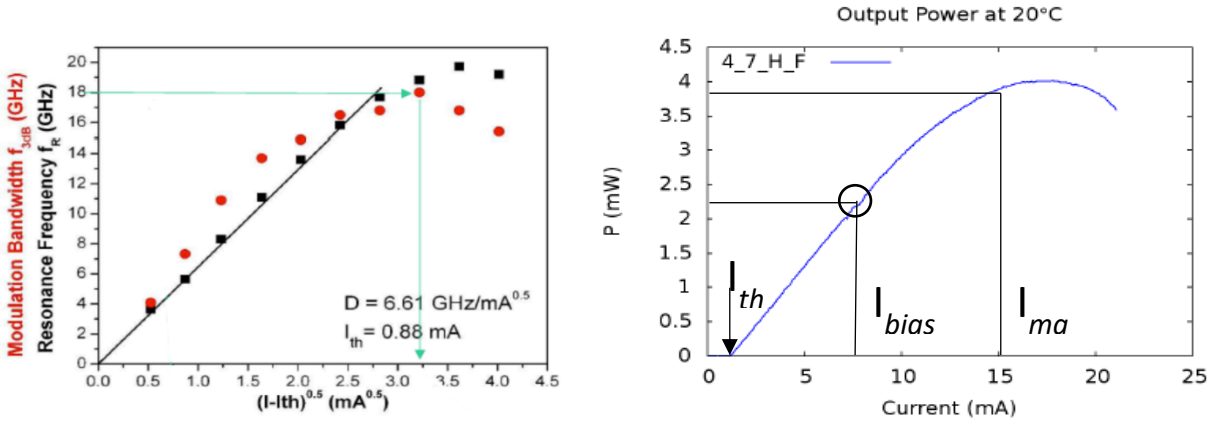

Figure 14 Modulation bandwidth (red circle) and resonance frequency (black square) as a function of the Ibias. Maximum bandwidth is achieved at I_{bias} of about 8 mA, corresponding to $(I-I_{th})^{0.5}$=2.64 (I_{th}=1 mA).

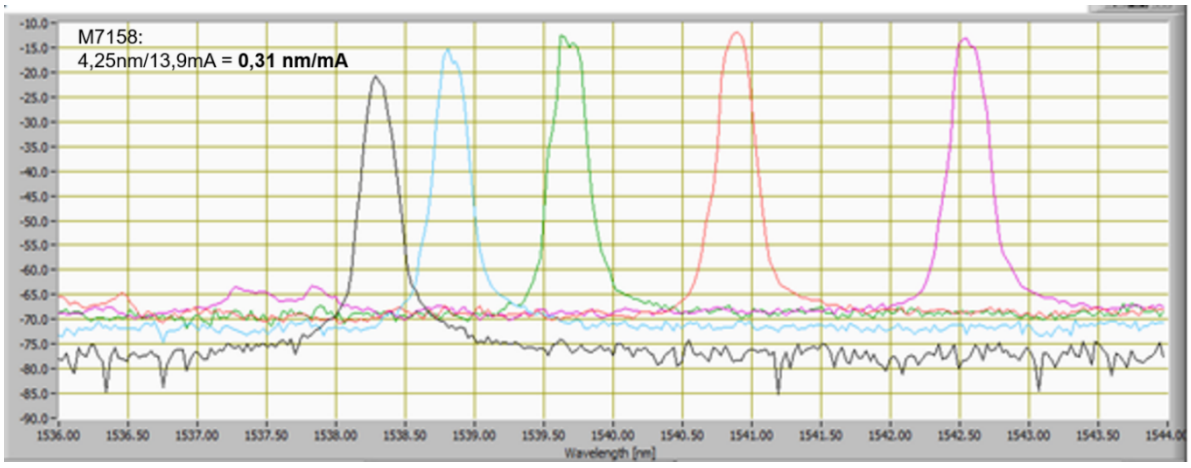

Figure 15 C-Band VCSEL emission tuning by means of the bias current.

4.2 VCSELs AND DRIVERS INTEGRATION

Regarding the PIC integration, for thermal reasons VCSEL drivers have been put outside the SiPh PIC, but still at short distance (<4mm) from VCSELs, allowing short wire bond (WB) for interconnections, as shown in Figure 16 (right). However, for high-speed and high bandwidth operations WBs have to be as short as possible (preferably <200μm). The design of the PIC with 10 VCSELs put on each side allows to achieve the VCSELs positioned as close to the PIC edge as possible.

With this architecture, the channel pitch, which is the physical spacing between the adjacent channels on any given edge of the chip, influences the chip size. In fact, the channel pitch is

dependent on the pitch among the following elements: the multiplexer input arms, the VCSELs, and the drivers. Consequently, the maxima of these elements decide the final pitch. We need thus VCSEL driver dimension to not exceed the range of 1.5-2 mm. In our realization, the channel pitch value is 2 mm, hence taking into consideration that some additional space is needed for the output fibre placement, the achieved chip size is around 20 x 20 mm^2.

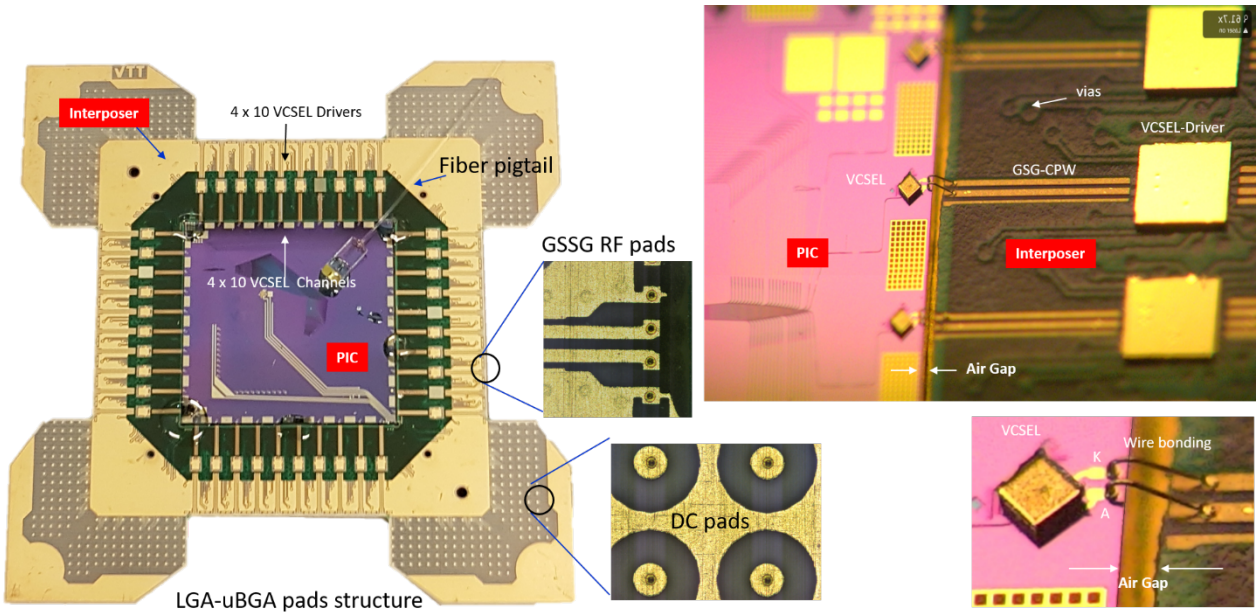

Figure 16. Tx MOD integration scheme: integration of VCSELs and drivers on a 20x20 mm^2 PIC (left). VCSEL flipchip bonded and interconnected (wire-bonding) to Interposer (right). A precise air gap is observed to thermally decouple PIC since working at constant temperature from heat generated by VCSEL Drivers.

4.3 THERMAL MANAGEMENT DESIGN

The thermal management of the Tx MOD consists in a set of engineered solutions aimed to extract different amount of heat at different temperatures in an efficient and repeatable manner.

The 100-GHz 1 x 40Ch AWG integrated on a SiPh PIC for the WDM channels multiplexing suffers of a natural shift $\Delta\lambda/\Delta t$ of approx. 0.07nm/degC. Therefore, a thermal change of approx 11 degC would be able to shift the entire AWG spectra of $\pm$ 1 channel. In practice, variations of just 1-2 degC are capable to create critical channel multiplexing instabilities. Moreover, up to 40 VCSELs have to be flip-chip bonded on top of the Si-PIC and interconnected to their corresponding drivers. For VCSELs, a typical wavelength vs temperature sensitivity $\Delta\lambda/\Delta t =$ 0.01nm/degC has been considered. To maintain stable the PIC temperature when in operation, a standard passive heatsink is therefore not adequate. Hence an active-cooling solution provided by a Thermo-Electric Cooler (TEC) having a cold face acting as an "infinite" black body, has been used. For integration reasons the TEC module is not embedded into the Tx MOD, but externally mounted into an evaluation or customer board instead.

On the other hand, the heat generated by 40 VCSEL drivers should not overload the TEC functionality but it should be conveniently dissipated instead through a conventional passive heatsink system. This is because these microelectronic ICs can withstand with large operating temperature variations **Δt =Rt ± 30** degC (or greater), with minimum impairment.

In PASSION, to finalize the Tx MOD thermal management, two distinct thermal paths have been conceived with the purpose to efficiently separate the active heat generated by VCSELs on PIC from a much larger heat amount generated by VCSEL drivers. (Figure 17)

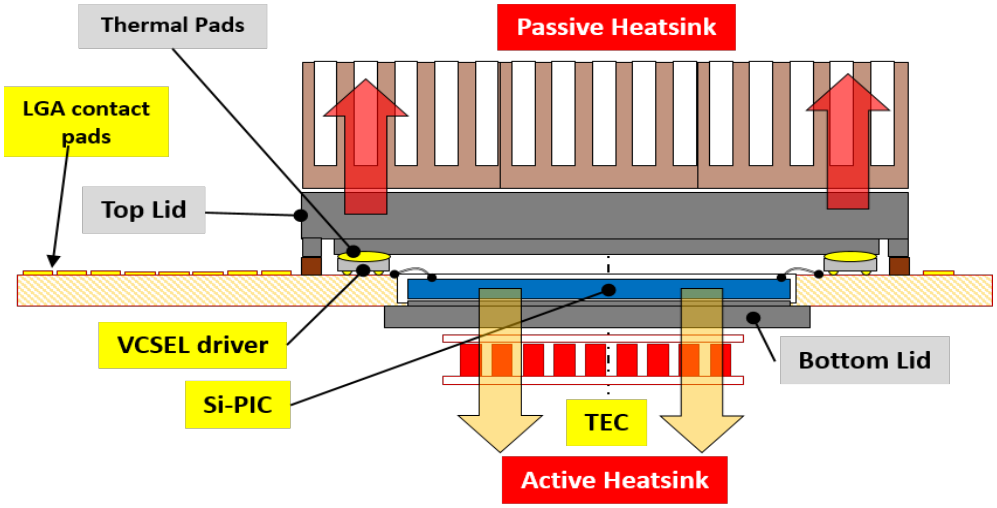

Figure 17 Thermal Model with 2 separate thermal paths.

In Table 2 are listed the operating conditions and the design margin assumptions of the Tx MOD heat sources.

Table 2 Tx MOD operating conditions

Devices	Conditions	Assumptions	Max Dissipated Power (W)
VCSELs	P_{VCSEL} = (≈1.7V $_{FW}$ x 15mA I_{max}) ≈0,0255 W	For design margin purpose only, P_{VCSEL} is considered totally converted in heat (although an approx 4mW is converted in optical beam)	0,0255W x 40 ≈ 1.02W
Drivers	$P_{Drivers}$ ≈0.23W/Ch	For design margin purpose only, the total amount of P_{DRIVER} is considered with all 40 drivers in full operation	0.23W x 40 ≈ 9.2W
TEC	P_{TEC} = (≈0.81A I_{tec} x 4.36 V_{tec}	Includes approx 0.2W of passive heats absorbed by TEC from ambient and prevalently from VCSEL Drivers due to not ideal thermal insulation gap between PIC and electrical Interposer	≈3.54Wmax

The thermal model, built in COMSOL, shows isothermal maps of the two separate thermal paths in Figure 18. In particular for each VCSEL bonded on a PIC, a temperature gradient between the

bottom side of the PIC (connected to TEC cold face =20degC through a bottom lid having 0.1Cdeg/W thermal resistance) and the VCSEL DBR region has been reported to be 1.3degC.

Similarly, the VCSEL driver bonded on the Interposer and thermally connected to a suitable passive heatsink, by means of a Thermal Pad (thermal conductive elastomer having 4degC/W thermal resistance) shows a temperature gradient of approximately 40degC (from 20 ÷ 60 degC).

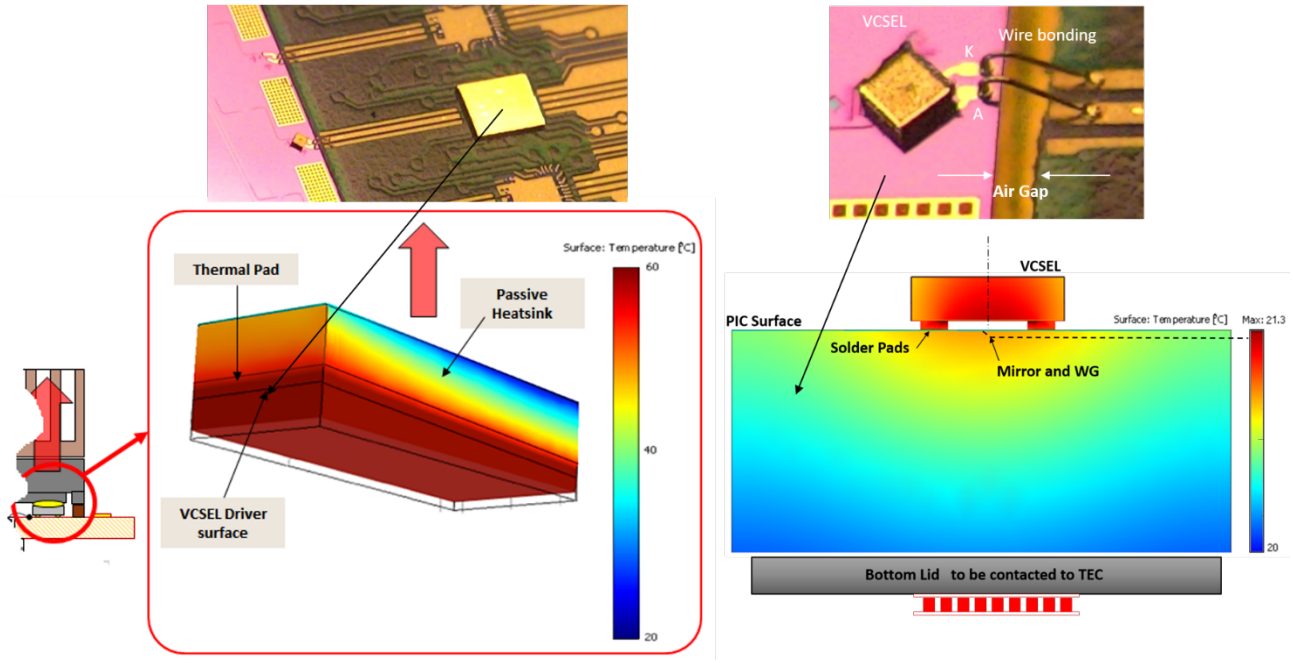

Figure 18. Temperature gradient between the bottom side of the PIC and the VCSEL DBR region for the VCSEL bonded on a PIC, achieved by COMSOL.

	Layer	Min	Max	Nom.	Tol-	Tol+	Thickness (Millimeter)	Stackup Picture TopLayer ep / ep	Family	Description	Type
	smffr						0,0200		Soldermask screenprinting	SM screenprinting	
	epfr	0,0130	0,0270	0,0200	0,0070	0,0070	0,0200		Cu	2µ + 18µm	MIXED - Foil
							0,0376		R-5680	1027 (0049)	
	ip2	0,0100	0,0250	0,0190	0,0090	0,0060	0,0220		Cu	5µ + 17µm	MIXED - Foil
							0,0505		R-5680N	1035 (0060)	
	ip3	0,0100	0,0250	0,0190	0,0090	0,0060	0,0220		Cu	5µ + 17µm	POWER_GROUND - Foil
							0,0345		R-5680N	1035 (0060)	
	ip4	0,0100	0,0350	0,0290	0,0190	0,0060	0,0290		Cu	18µ + 14µm	SIGNAL
							0,0500		R-5785	0050	
	ip5	0,0100	0,0350	0,0290	0,0190	0,0060	0,0290		Cu	18µ + 14µm	SIGNAL
							0,0351		R-5680N	1035 (0060)	
	ip6	0,0100	0,0250	0,0190	0,0090	0,0060	0,0220		Cu	5µ + 17µm	MIXED - Foil
							0,0477		R-5680N	1035 (0060)	
	ip7	0,0100	0,0250	0,0190	0,0090	0,0060	0,0220		Cu	5µ + 17µm	MIXED - Foil
							0,0365		R-5680	1027 (0049)	
	epba	0,0130	0,0270	0,0200	0,0070	0,0070	0,0200		Cu	2µ + 18µm	MIXED - Foil
	smfba						0,0200		Soldermask screenprinting	SM screenprinting	
				0,1550			0,5178	Total Thickness (Calculated)			
				0,1550			0,5120	Over Mask (Customer)	+0,1000	-0,1000	

Figure 19. Interposer Structure made with 8 layers of Megtron 7.

4.4 RF DESIGN AND WIRE BONDING

In the Tx MOD electrical design, the routing of all RF lines on the Land Grid Array (LGA) Interposer posed several challenges in definition of all Redistribution Layers (RDLs). An overview of the Interposer´s structure is shown Figure 19 where 8 layers of Panasonic-Megtron7 (Laminate R5785 and Prepreg R5680 having dielectric constant Dk 3.4@12GHz and dissipation factor Df 0.002) have been used to interconnect all drivers to VCSELs and to LGA-μBGA contact pads. The most challenging part was to rout all 100-Ohm Differential Ground-Signal-Signal-Ground (GSSG) with a total amount of 160 routed lines. Furthermore, additional 120 Single Ended lines in 50-Ohm Ground-Signal-Ground (GSG) configuration have been designed to interconnect the driver output pads to the corresponding VCSELs (Figure 20).

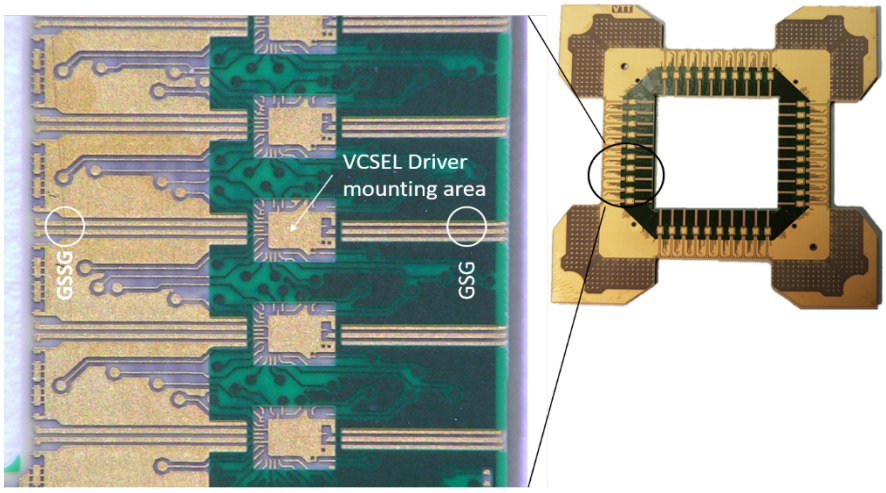

Figure 20. Overview of the Interposer´s RF routing lines with 100-Ohm Differential Ground-Signal-Signal-Ground (GSSG) CPW for the VCSEL driver input side and a 50-Ohm GSG CPW toward the VCSEL wire bonding pads.

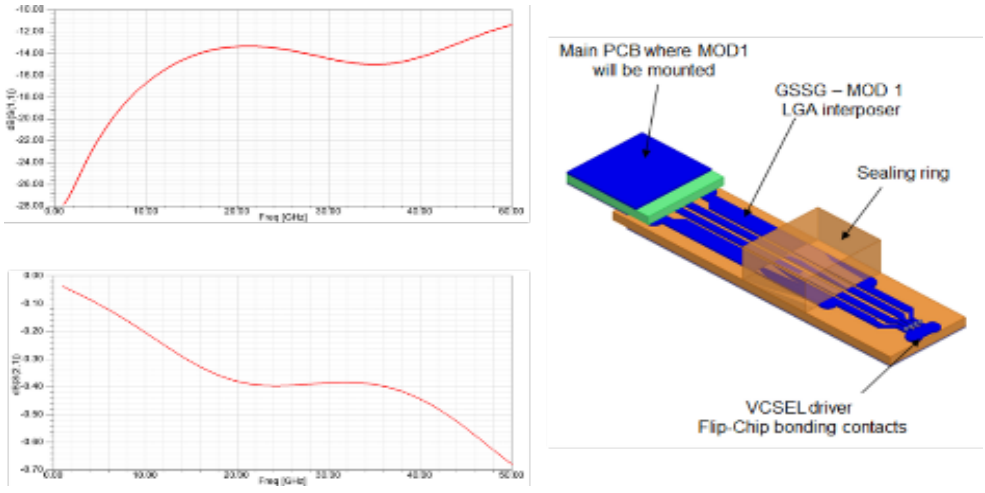

Figure 21. Simulated Return and Insertion Loss of the GSSG lines.

Simulated S_{11} and S_{21} coefficients of the GSSG input lines, are reported. The S_{11} (return loss) is about -14dB and S_{21} (insertion loss) is about 0.4 dB up to 45 GHz of analog bandwidth (Figure 21). Both are considered satisfactory for a good LGA Signal Integrity behavior at bit rates >25Gb/s.

Also relevant was to model the wire bonding RF performance between VCSEL´s pads and the Interposer. In the actual Tx MOD assembly a loop of 500μm and a total air-gaps of 150μm have been measured. The S-parameters include contributions also from the CPWs (Figure 22).

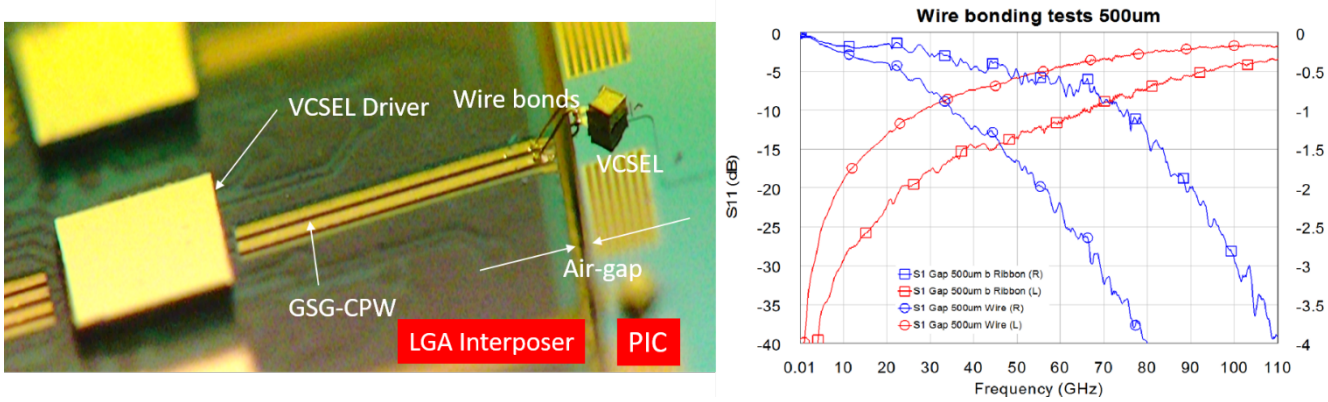

Figure 22 S-parameters of 500μm Wire Bonding loops and 150μm air-gap have been modelled and measured.

5 CONCLUSIONS

In this deliverable, an overview of the most important integration milestones related to the VCSEL-based SiPh PIC constituting the PASSION Tx MOD have been provided. In the project development we directly moved to the design and realization of a single integrated 40-VCSEL PIC, thus we have considered the co-integration of VCSELs within the whole Tx MOD PIC, and not only the 10-VCSEL sub-module.

The PIC design now includes a 1 x 40CH 100GHz-spaced AWG fabricated with a VTT 3μm SOI process. VCSELs have been successfully flip-chip bonded on PIC. The light coupling tests are also performed to evaluate the up-reflecting mirror solution. The thermal management design has been also described with emphasis on the two separate heat flow routing and dissipation concept and related thermal models.

We have demonstrated that the full integration phases of the PASSION Tx MOD have been completed and that also the wire-bonding interconnections between driver and VCSEL have been performed.

REFERENCES

[1] G. Delrosso et al., “Development and scalability of a 2 Tb/s data communication module based on a 3 µm SOI silicon photonics platform” in 22th International Conference on Transparent Optical Networks (ICTON), IEEE CONFERENCE PROCEEDINGS 2020, pp. 1 – 4 (2020).

[2] P. Parolari et al., “Preliminary assessment of photonic solutions based on C-band VCSELs for multi-Tb/s metro networks” in 22th International Conference on Transparent Optical Networks (ICTON), IEEE CONFERENCE PROCEEDINGS 2020, pp. 1 – 4 (2020).

ACRONYMS

4-PAM 4-level pulse amplitude modulation
AWG Arrayed Waveguide Grating
BTJ buried tunnel junction
DMT discrete multitone
EG Echelle Gratings
E/O electro optical
GSSG Ground-Signal-Signal-Ground
GSG Ground-Signal-Ground
IL insertion loss
LGA Land Grid Array
MCF multicore fibre
MM multi mode
MOD module
MUX multiplexer
PDM polarization division multiplexing
PIC Photonics Integrated Chip
RF radio frequency
RDL redistribution layers
S-BVT sliceable bandwidth/ bit rate variable transceiver
SiPh silicon-photonics
SM single mode
SOI Silicon-Over-Insulator
TEC thermo-electric cooler
TIR total internal reflection
Tx transmitter
VCSEL vertical cavity surface emitting laser
WB wire bond
WDM wavelength division multiplexing
WLT wafer-level testing