PHOTONICS PUBLIC PRIVATE PARTNERSHIP

D4.7 - HYBRID INTEGRATED LOW INSERTION LOSS DISAG/AGGREGATOR

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EXECUTIVE SUMMARY

This report corresponds to the deliverable D4.7 of PASSION project and relates to hybrid integration of Silicon Photonics (SiPh) and Indium phosphide (InP) material platform exploited for the first time for switching circuit concepts.

VTT in collaboration with the partner institution TUE has developed an integrated wavelength selective switch (WSS) on a 3-μm SOI platform to be used in an add/drop path of a switching node; The device provides demultiplexing functionalities with a wavelength-blockers (WBL) design, 1x12 channel arrayed wavelength gratings (AWGs) with 100 GHz channel spacing and an FSR of 2 THz. Two photonic integrated circuit (PICs) centered at 1546.51 nm and 1546.71 nm have been designed, fabricated and characterized. A specific InP chip integrating 12 SOAs has been developed at TUE, each semiconductor optical amplifier (SOA) under proper electrical control behaves as a switching element either becoming loss-less transparent or heavily wavelength absorptive, accordingly to the applied bias voltage.

Aiming to realize a low loss hybrid integrated WBLs and leveraging on hybrid integration capabilities offered by VTT SOI platform, InP SOA chips have been conceived to be flip-chipped into lithographically-defined cavities, obtained in the SiPh chip. This approach also provides electrical connections and probing pads for external driving controls.

In-cavity special vertical hard-stoppers in Silicon along the three edges of the cavity with exception of the top edge, in a horse-shoe configuration, have been obtained allowing SOAs to stop in position during flip-chip bonding with very high accuracy. To improve and simplify the optical coupling scheme, and additional U-shaped passive WG on SOAs has been additionally added, favoring the launch IN/OUT of optical signals aimed to maximize the optical couplings during the flipchip bonding process.

Functional description and E/O characterization of the Multicast Switch (MCS) as well as the WLB have been reported.

The presented solutions and results represent a technological advancement in switching design especially for low cost HL4 node level. WLB with 50-GHz granularity performed by reliable AWGs design integrated on a SiPh PIC have been demonstrated.

Further improvements to maximize both SOA´s switching time and gain characteristics while overcoming extra losses would be needed and currently addressed.

1 INTRODUCTION

The purpose of this deliverable relates to hybrid integration of SiPh with InP devices (SOAs) exploited for the first time for switching circuit solutions. In particular a WSS with WBL obtained on a SiPh PIC with hybrid mounted InP SOAs has been designed, fabricated and tested. The following sections will provide an overview of the design and the E/O characterization performed on two WBL chips.

2 DESIGN OF A SIPH ADD/DROP WSS PIC

VTT in collaboration with the partner institution TUE has developed an integrated WSS on a 3-μm SOI platform to be used in an add/drop path of a switching node. As thoroughly explained in D2.3 [1], the switching architecture is based on *broadcast-and-select* scheme, in which the signal is broadcasted by a *1*x*m* splitter and is selected by *m* WBLs at the output ports.

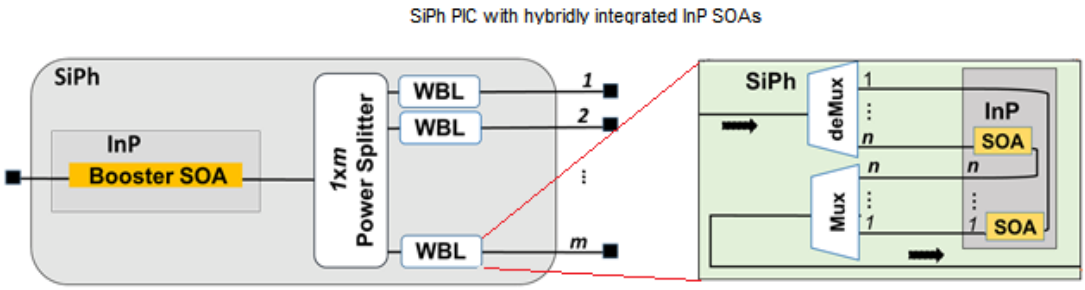

Figure 1. Hybrid WBL for WSS in an add/drop path

For the first time the purpose of this hybrid integration is to exploit a 3-μm SOI platform [2] with InP SOA switches to enable loss-less or very low-loss switching performances.

The WBL is constituted by de-multiplexing/multiplexing (DeMux/Mux) circuitry on SiPh and InP SOA switching gates as illustrated in Figure 1. The hybrid WBL is based on SiPh DeMux/Mux circuits and SOA switching gates on InP chip. The integration scheme used cavities on the SiPh chip to flip-chip bond the InP chips after fabrication. Currently, this circuitry is under test.

With the aim to achieve the (de-)MUX functionality within the WBL design, 1x12 channel AWGs with 100-GHz channel spacing and an FSR of 2 THz, centered at 1546.51 nm and 1546.71 nm have been designed on the VTT 3-μm SiPh platform [2].

Typical characteristics for the same design, centered at 1550 nm, is shown in Figure 2(a), and the chip image of the implemented design for the deMUX-SOA switch-MUX configuration is shown in Figure 2(b). The input light, consisting of several wavelength channels, is demultiplexed by the first AWG into their component wavelengths with 100-GHz channel spacing. These individual wavelength outputs of the first AWG are fed as input to the wavelength blocking element – the InP SOA chip. Each of the 12 SOAs can be, individually, either be turned on by pumping them to transparency, or kept off by not biasing them in which case they absorb the wavelength. The output of all the SOAs

is further collected as input by the second AWG, and multiplexed into a single output that is collected as the output of the SiPh chip. Thus, individual channels can be either passed forward, or blocked selectively, with the help of this hybrid wavelength blocker [3].

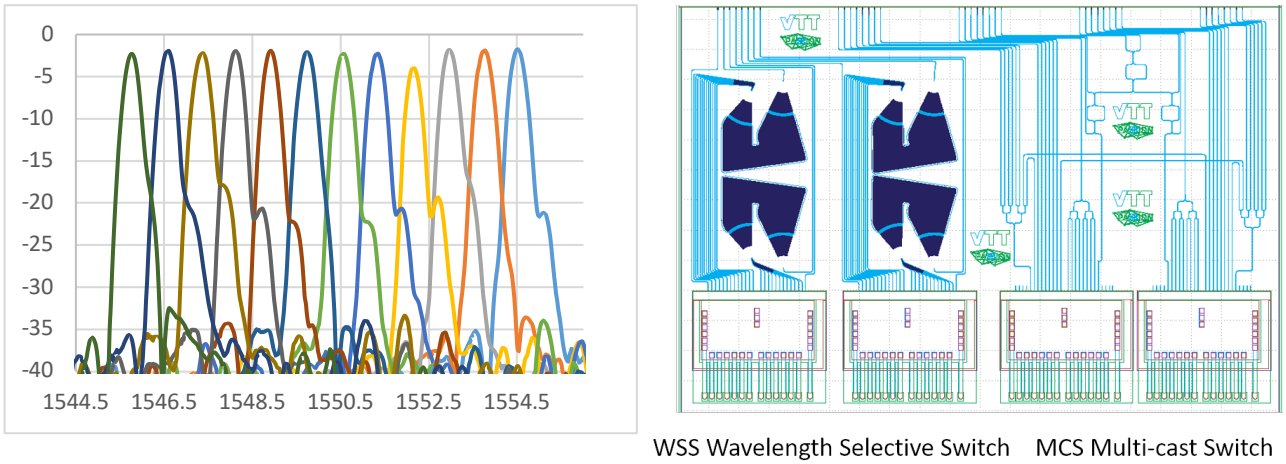

Figure 2 (a) Typical optical spectra of the 1x12ch 100GHz de-MUX AWG , (b) chip image of the actual deMUX-SOA switch-MUX configuration

2.1 SiPh Cavity design for InP SOA chip hybrid integration

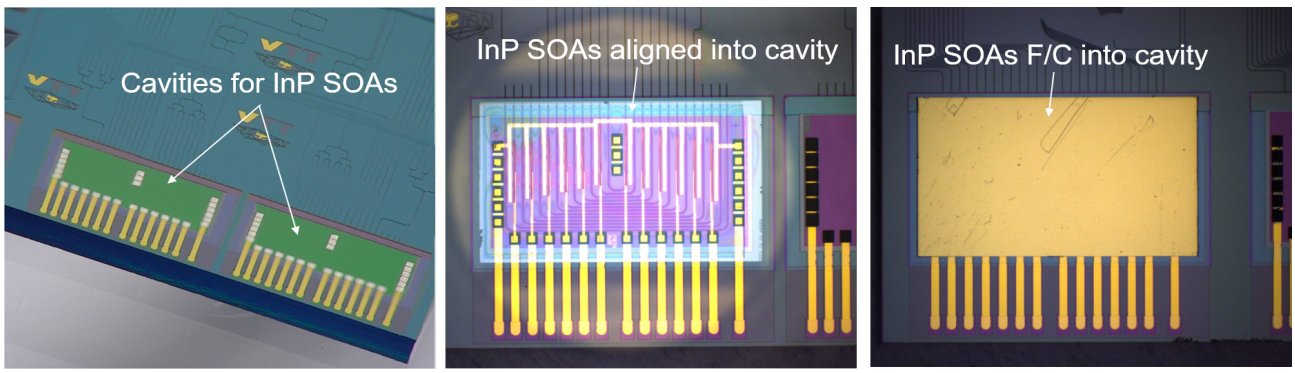

Figure 3 Precision cavities obtained on PIC and InP SOA aligned and flip-chip in position into cavity

With the hybrid integration concept, the idea is to have all the passive optical components plus the electrical wiring on the SiPh platform and the SOA actives are implemented on the InP platform. This would necessitate back and forth optical power coupling between the SiPh and the InP platforms. This, in turn, translates to a very good waveguide optical axis alignment between the two platforms. Since both of them have their waveguides at the top of their respective chips, achieving such alignment would require the InP chip to be flip-chipped down into a precisely defined cavity in the SiPh chip. In addition, the integration scheme should also provide electrical connections and probing pads for pumping the SOA where necessary. A well-defined cavity in the SiPh chip that complements the InP chip in physical geometry, optical design, and electrical connections is necessary in order to realize a low loss hybrid integrated WBL.

As shown in Figure 3, the first requirement is that the SiPh waveguides from the (de-)MUX complement the InP waveguide design when the InP SOA chip is flip-chipped down during assembly. This means that the SiPh waveguides need to be a mirror image of the InP waveguides. This is accomplished within the SiPh design and defines the top end of the SiPh cavity. This top edge of the cavity, far away from the waveguide area, is designed to physically contact the InP chip such that a gap of 100 nm remains between the two waveguide sets. Thus, they act as horizontal stoppers for the two waveguide sets avoiding crashing into each other. In addition, the cleaving tolerance of the InP chip is ±20 µm, which means the cavity has to be wider by a margin of, at least 40 µm, on each side to accommodate the InP chip.

For designing the cavity depth at different points, several vertical positions with respect to a reference, are to be taken into consideration for both the InP and the SiPh chips: the waveguide optical axis, the top of the metal pads and antireflection (AR) coating layer, and the surfaces that come in contact during integration. In addition to this, the bonding technique utilized for the integration can play a role. Low loss optical coupling between the two chips needs very accurate vertical alignment between the two optical axes, and this is accomplished by defining vertical hard-stoppers during the fab. This has the added advantage of relaxing the height tolerance during the integration itself and allows for a flexible integration technique such as tin (Sn) solder bonding to be utilized for the purpose. Taking all factors into consideration, the vertical hard-stoppers are defined at the three edges of the cavity (except the top edge) in a horse-shoe configuration, with several openings at the back edge for allowing the electrical routing lines to connect to the probe pads, as shown in Figure 4. They are defined by the InP surface making contact with the partially etched buried oxide of the SiPh chip and the choice is made based on their accuracy as a vertical reference, their inflexibility, and flatness.

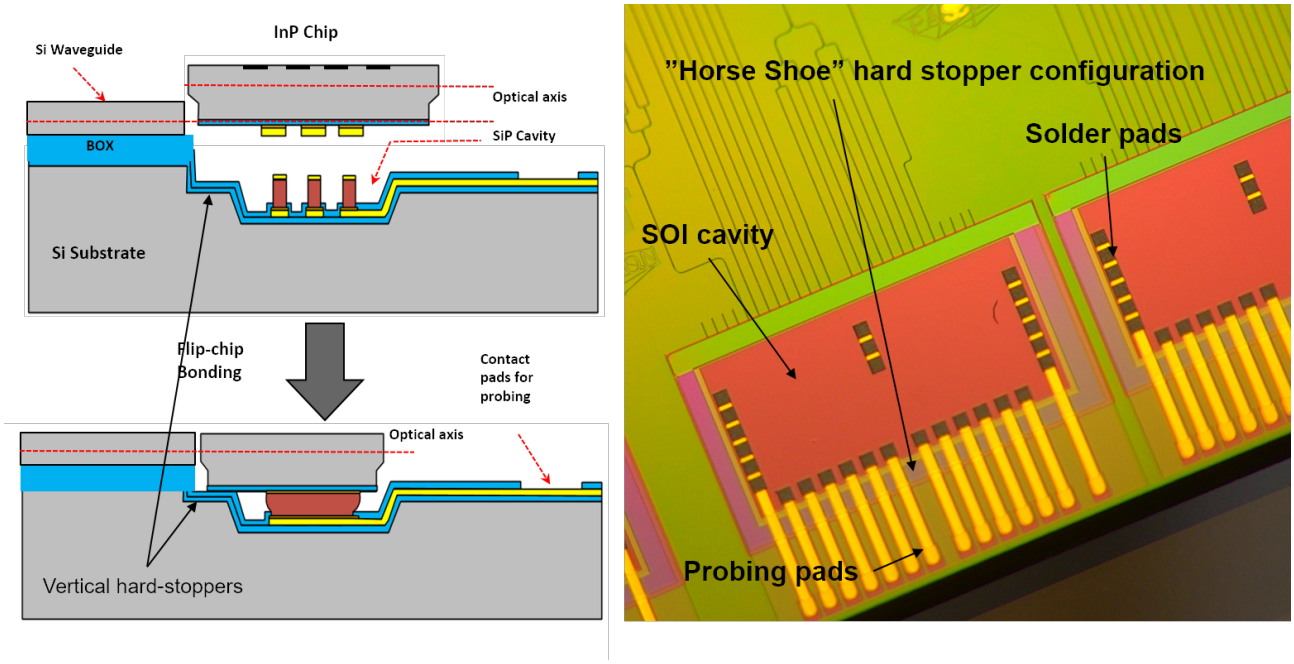

Figure 4 Vertical hard-stoppers defined at three edges of the cavity in a horse-shoe configuration

VTT has assembled four InP chips on SiPh platform as shown in Figure 5(a). In Figure 5 (b) the used measurement setup is depicted. The optical light coupling is performed by using lensed fibers with mode field diameter (MFD) of 2.5 μm which are mounted on a 3-axis alignment stages. The temperature of the chip is kept at 20^{0}C during the measurement. The current source is used to drive SOA for enabling the switch capability of the hybrid circuits.

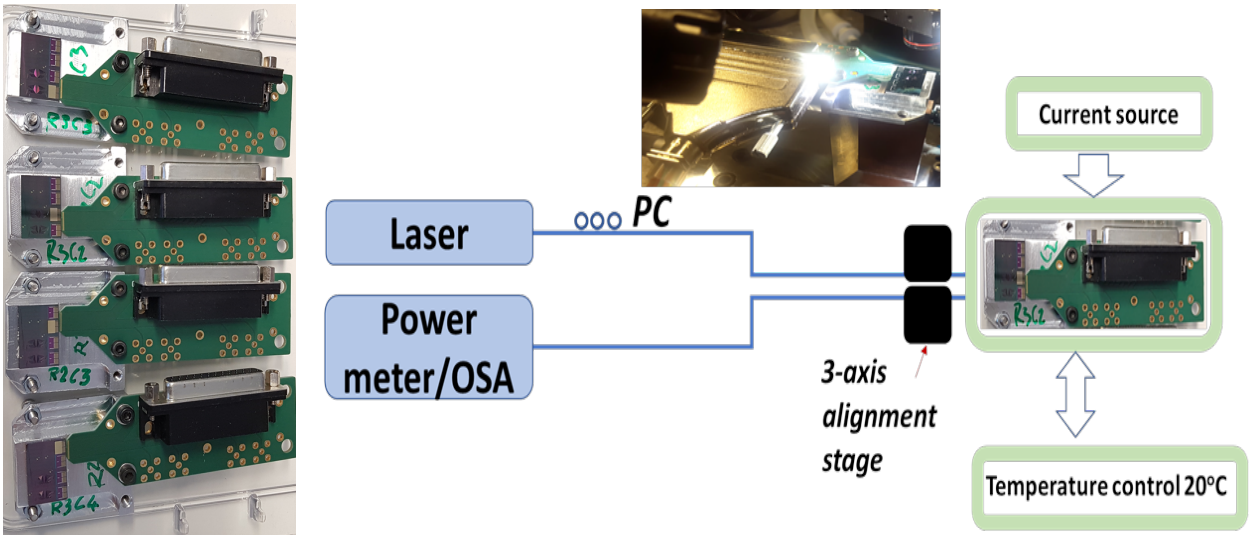

Figure 5 (a) the 4 SiPh chips and integrated InP SOAs interconnected to a test PCB, (b) Measurement set up for SiPh chip characterization

The names and circuit functionalities are summarized in Table 1. Two of the assembled chips are hybrid WBLs and two of the assembled chips are MCS switches.

Table 1 Chip name and functionality

Name of circuit	R3C3	R3C2	R2C3	R3C4
Cavity # in SiPh chip	1	2	3	4
Functionality	WBL	WBL	MCS	MCS

2.2 FUNCTIONAL DESCRIPTION OF HYBRID WBL

The schematic representation of the hybrid WBL assembled in circuits R3C3 and R3C2 is shown in Figure 6 and Table 2. The WBL has 12 channels, therefore the deMux/Mux AWG has 12 output waveguides. Similarly, the InP chip contains 12 SOA gate switches designed in a U-shaped waveguide structure. The hybrid functionality of the WBL is based on the coupling of light between SiPh and InP on the waveguide facets labeled as [f1, …, f24]. A WDM input signal to the hybrid WBL first passes through the deMux circuit which separates the signals into individual wavelengths Ch1, … Ch12. The individual wavelengths then are coupled into SOAs on InP chip, through the waveguide facets numbered [f1,..f12] between SiPh and InP. The individual wavelengths are either passed or blocked by the SOA switching gates in the InP chip. The switched signal is then coupled back into SiPh chip through the interfaces [f13, … f24].

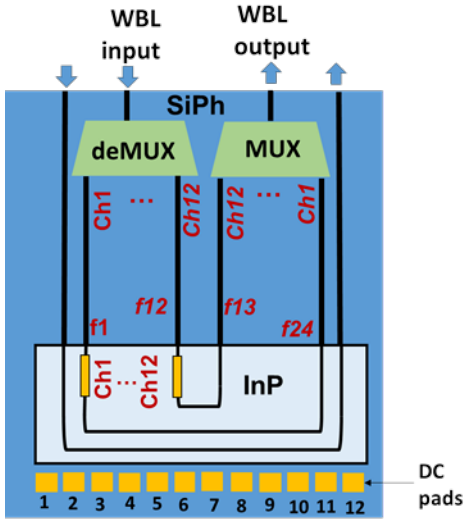

Figure 6 Block diagram of hybrid WBL

Channel	Facet	(DC pad #)
Ch1	[f1,f24]	1
Ch2	[f2,f23]	12
Ch3	[f3,f22]	2
Ch4	[f4,f21]	11
Ch5	[f5,f20]	3
Ch6	[f6,19]	10
Ch7	[f7,f18]	4
Ch8	[f8,f17]	9
Ch9	[f9,f16]	5
Ch10	[f10,f15]	8
Ch11	[f11,f14]	6
Ch12	[f12,f13]	7

Table 2 DC Pads with corresponding optical channels

In addition, a completely passive U-shaped waveguide as shown in Figure 7 is coupled through facets f0, and f25 between the SiPh and InP chip. This serves as a baseline to characterize the coupling efficiency of the hybrid integration. Within the WBL a total of 26 SiPh-InP coupling take place through facets [f0,…,f26]. The relation of the WBL wavelength channel, with respect to the pair of facets and the SOA number, which is the same as the DC pad number on SiPh chip is reported in Table 2.

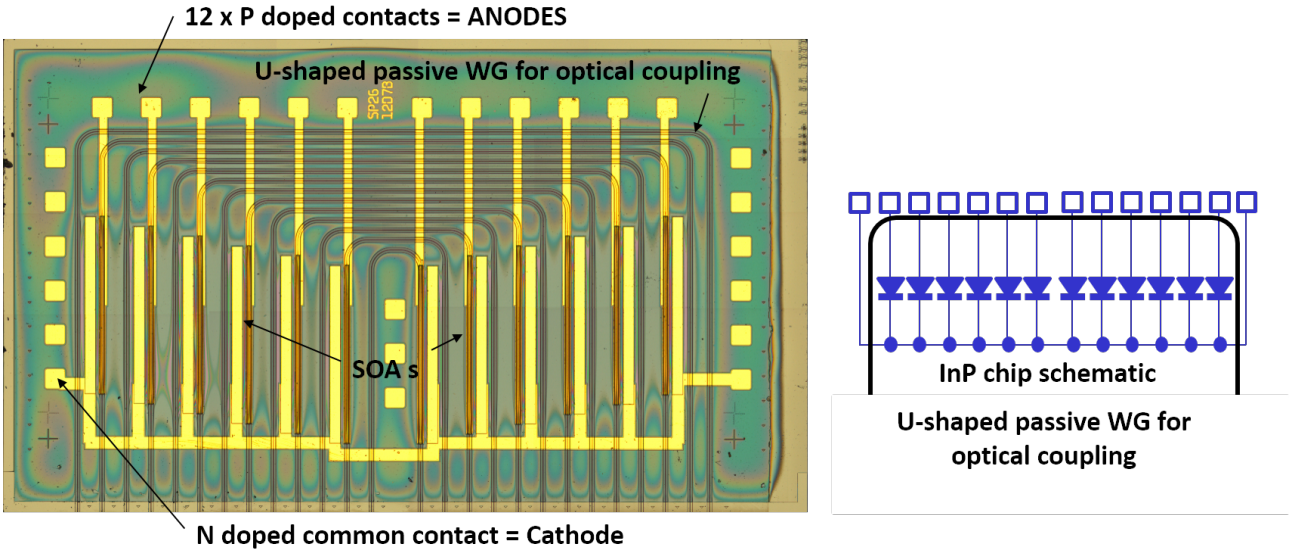

Figure 7. 12Ch InP SOA chip with U-shaped passive WG for optical coupling

2.3 FUNCTIONAL DESCRIPTION OF MCS

Hybrid multi-cast switching functionality is implemented via passive SiPh circuitry together with InP SOA arrays that serve as gate switches as illustrated in Figure 8. The circuit implemented 1x2 MCS functionality while emulating large scale integration (8x8 MCS) by accommodating extra input/output ports also known as broadcasted-inputs and broadcasted-outputs. Therefore, the 9 SOAs within InP are used: 1 SOA is used for boosting (amplification) and 8 SOAs are used as gate switches. The flip/chip (F/C) bonding of InP SOA arrays into SiPh circuitry has been performed at VTT.

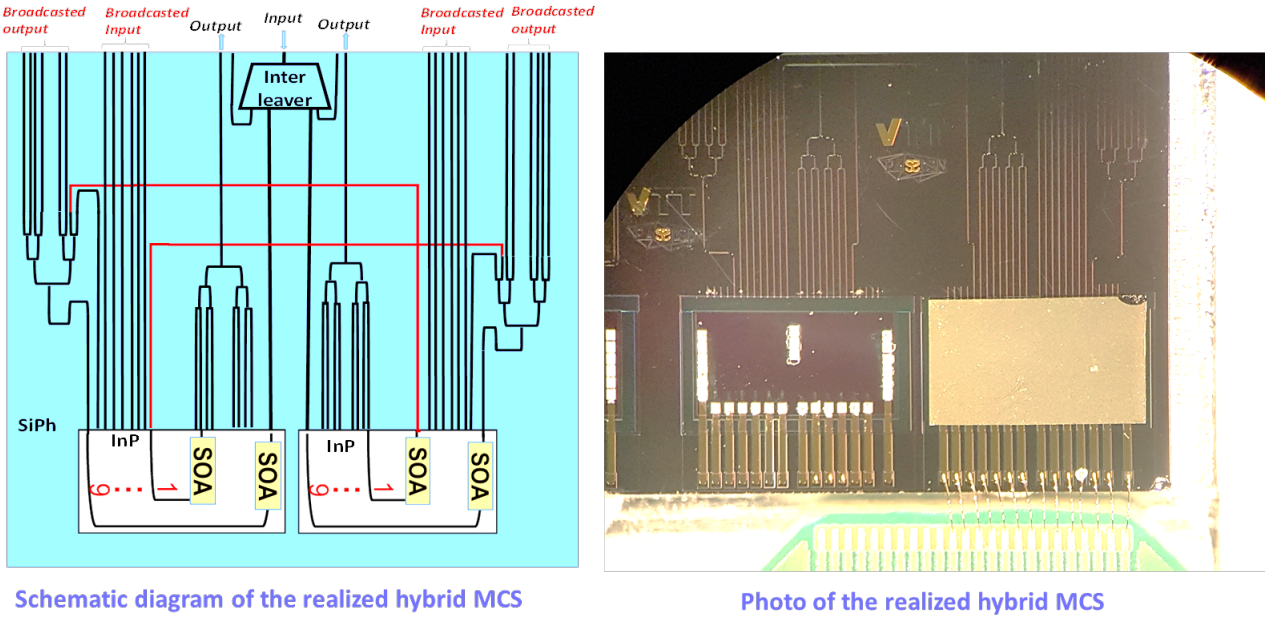

Figure 8. Schematic and photo of the realized hybrid MCS

3 WBL E/O CHARACTERIZATION

This section describes the E/O characterization of the 12 channel InP SOA chip F/C bonded on SiPh PIC. Due to the particular relevance and complexity the main objective of this deliverable is to perform the characterization of the WBL structure which includes both SOAs and wavelength multiplexing structures, on the other hand the MCS has just splitter/combining architectures whose characterizations is less relevant and is ongoing.

In particular the I-V curves and the insertion losses of the different assembled circuits have been measured, but assembly R3C2 allowed more measurements.

3.1 CHARACTERIZATION OF ASSEMBLY R3C3 (WBL)

The first measured PIC is the assembled circuit R3C3, which is hosted in the 1st cavity, as can be seen in the mask layout and in the assembled circuit shown in Figure 9(a) and (b) respectively.

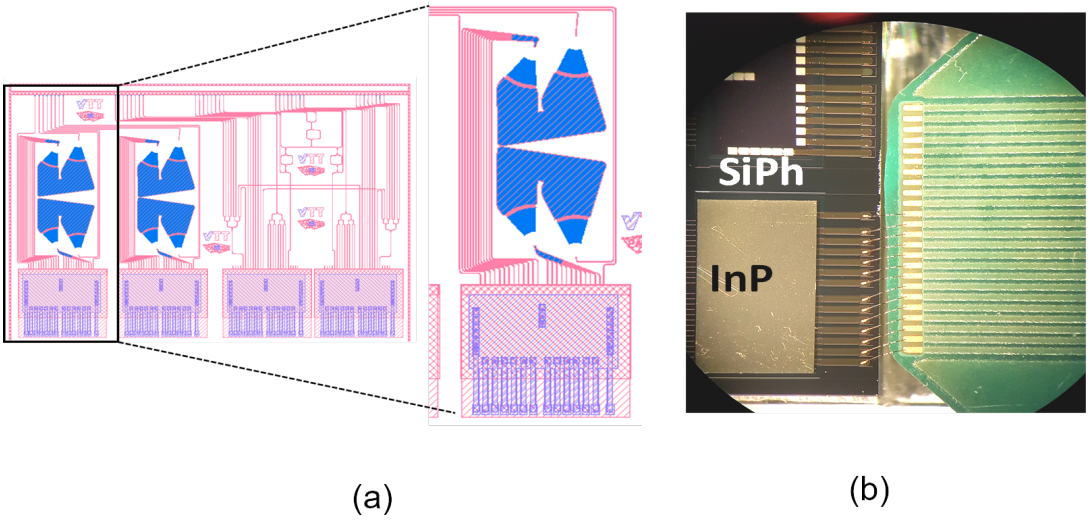

Figure 9. Assembled chip R3C3 (a) mask layout of SiPh chip with cavity (b) R3C3 F/C bonded in position

Table 3. Status of I-V characteristics SOAs in R3C3

SOA-number	1	2	3	4	5	6	7	8	9	10	11	12
I-V	NF	NF	NF	Open	Open	Open	OK	Open	Open	Open	OK	OK

3.1.1 I-V curve test

First, the I-V curve measurements were done on all the 12-SOAs, and 6 of the 12 SOAs show open circuit and are labeled as Open in the above Table 3. From the remaining 6 SOAs, the first 3 SOAs had a malfunctioning (named NF in Table 3), while 3 SOAs, namely SOA 7, 11, 12 show typical I-V curve of a SOA. SOAs 11 and 12 are at the edge of the InP chip, while SOA 7 is located in the middle of the InP chip. The 3 SOAs correspond to the WDM channels 2, 4 and 12 as shown in Table 2. Figure 10 presents the results of the measurements on the 6 SOAs.

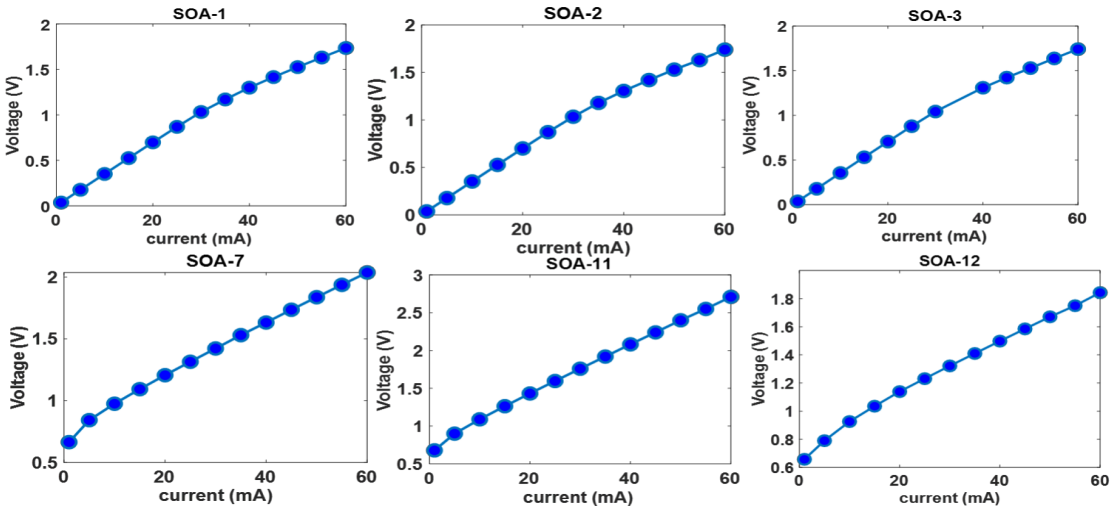

Figure 10 I-V curve tests after flip-chip bonding of R3C3

3.1.2 Insertion loss measurement

At first we measured the insertion losses through the U-shaped straight line, spanning the SiPh chip and InP chip, which were found to be 58 dB. Next the single insertion losses through SOA 7, 11, and 12 were measured by directly injecting the laser light. Table 4 shows the end-to-end insertion losses, while the gate SOAs are turned on. The hybrid coupling losses per SiPh/InP facet were then estimated by considering fiber-to-SiPh chip coupling loss, any excess loss in the fibers and gains of the SOA. After calibrating the measurement, with fiber-to-chip-coupling losses, excess loss in the fiber, and SOA gain, the hybrid coupling loss per facet is estimated to be 23.5 dB, 23.15 dB and 24.25 dB for channel 2,4 and 12 respectively.

Table 4 Insertion loss measurement of 3 operating channels: (*) Calibrated 3dB/facet coupling loss, 4 dB excess loss in the fibers, SOA gain)

SOA-number	7	11	12
SOA current (mA)	50	80	80
SOA gain (dB)	6	10	10
facet number	[f12, f13]	[f4, f21]	[f2, f23]
Channel number	12	4	2
End-to-end insertion loss (dB)	52.5	46.3	47
Estim. hybrid coupling loss/facet (dB) *	22.75	20.65	21.0

3.2 CHARACTERIZATION OF ASSEMBLY R3C2 (WBL)

The assembled circuit R3C2 is located in the 2nd cavity as can be seen in the mask layout shown in Figure 11(a) and (b) respectively.

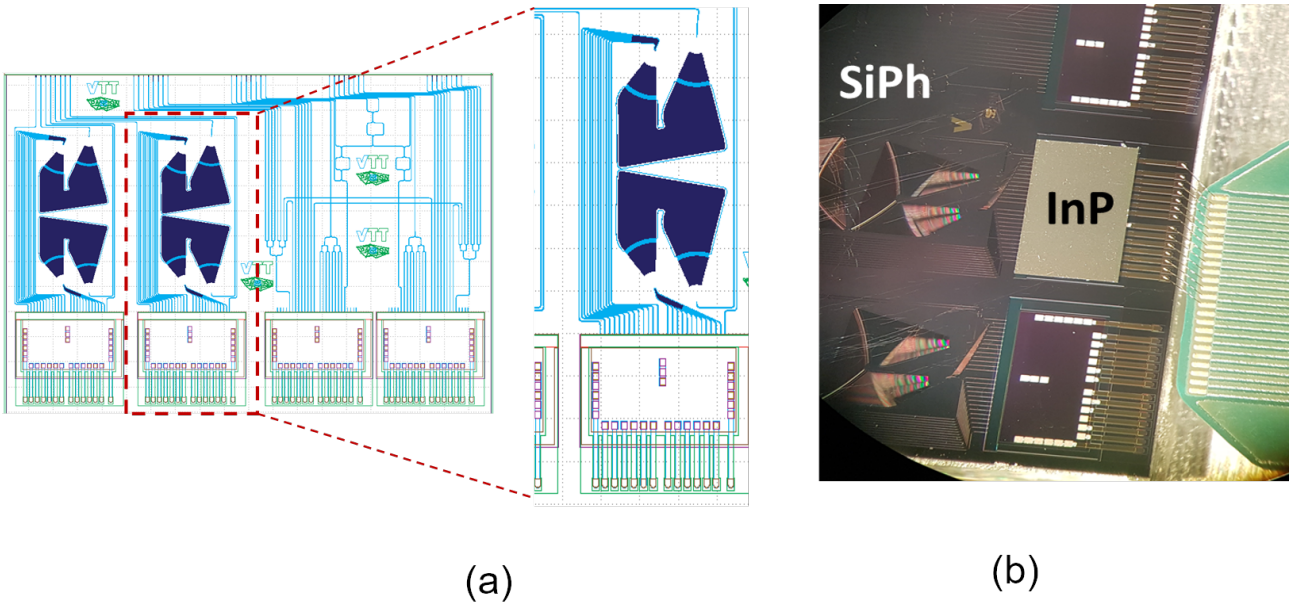

Figure 11 Assembled chip R3C2 (a) mask layout of SiPh chip with cavity (b) R3C2 F/C bonded in position

3.2.1 I-V characteristics

Table 5. Status of I-V characteristics SOAs in R3C2

SOA-number	1	2	3	4	5	6	7	8	9	10	11	12
I-V	Open	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK

Table. 5 shows the status of the I-V characteristics of the 12-SOAs after assembly in R3C2 chip, and standard I-V curve characteristics were measured for all SOAs except for SOA-1 which showed an open circuit.

The I-V curve measurements of the 11 operating SOAs before and after flip-chip bonding are reported in Figure 12(a) and Figure 12(b) respectively. The curves show a modest increment of resistance after bonding of about 4.5 Ohms.

3.2.2 Spectral measurement

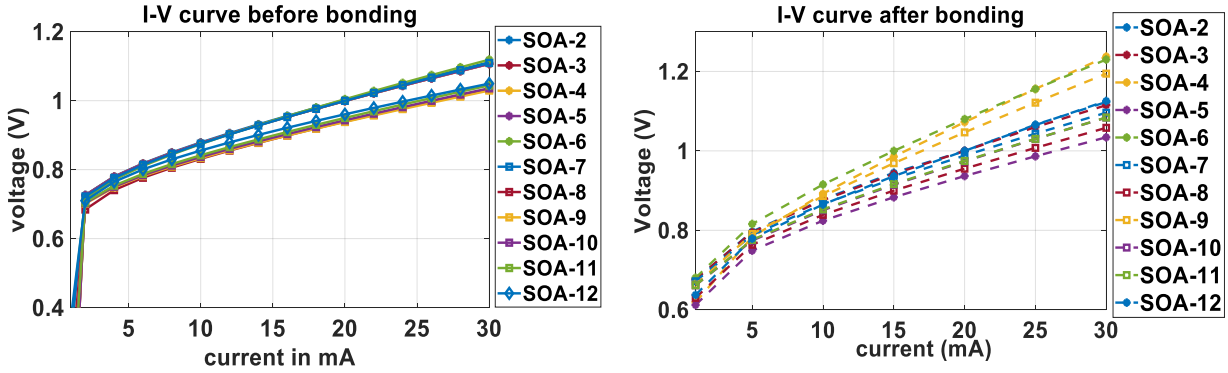

Figure 12 I-V curve measurements (a) before bonding (b) after bonding

The performance of the hybrid WBL is optically characterized by turning on the gate SOAs of each channel, where the wideband ASE output of the SOAs filtered by deMux/Mux AWG is collected at the input/output of the WBL. SOA-2, SOA-3, SOA-4, SOA-5, SOA-6, SOA-9, SOA-10, SOA-11, SOA-12 were turned on to take the spectrum measurements at input/output of the WBL as shown in Figure 13(a) and (b) respectively. Hence, the spectral profiles represent the de-MUX/MUX AWGs responses. A spectra overlapping of SOA-4 and SOA-5 is also shown, indicating that electrical paths of the SOAs have made undesired contacts during the flip-chip bonding process. Table.6 shows the channel central wavelengths of demultiplexing AWG (measured at the WBL input) and multiplexing AWG (measured at the WBL output). The central wavelengths of the deMux AWG and Mux AWG show a good match, which is important for the operation of the WBL and present the design channel spacing of 0.8 nm. For channels #3, the collected power at the deMux input is too low to measure the central wavelength. Furthermore, the AWGs are designed to have polarization insensitive performance which is confirmed by ASE spectral profiles. Channel #1 and # 12 were not in operation.

Table 6 Central wavelengths and channel number of hybrid integrated WBL

De MUX center wavelength (nm)	1544.8	NA	1546.3	1546.97	1547.9	1548.61	1549.48	1550.2	1551	1551.75
MUX center wavelength (nm)	1544.75	1545.55	1546.35	1547.1	1547.9	1548.67	1549.5	1550.25	1551.2	1552.03
Channel #	2	3	4	5	6	7	8	9	10	11
SOA #	6	8	5	9	4	10	3	11	2	12

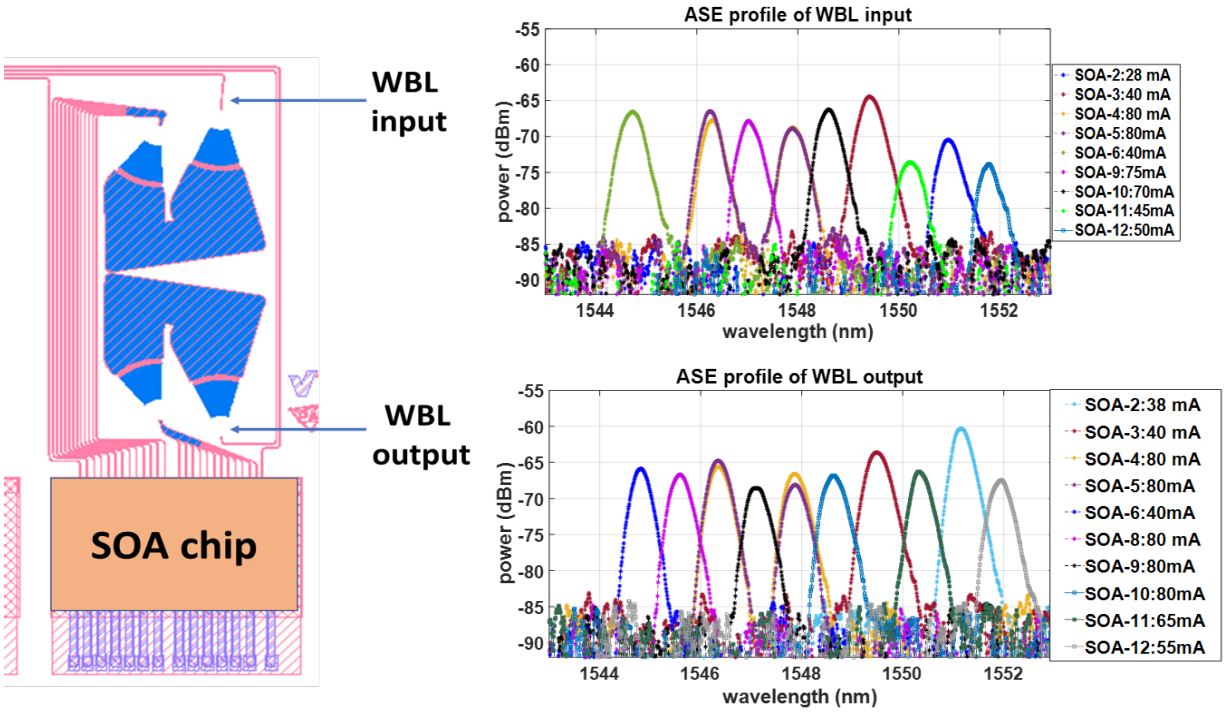

Figure 13 Spectrum measurement (a) measured at WBL input (b) measured at WBL output

The SOAs are tuned at different current values to minimize lasing observed in the SOAs. Lasing effects could be originated by reflection at facets where SiPh and InP chips are interfaced. The manual process of polyamide removal might have compromised the quality of anti-reflection (AR) coating on InP SOAs thereby increasing reflection and initiating lasing. Table. 7 lists the threshold current (mA) before lasing fringes are observed in the output spectrum. Due to the varying degree of reflection happening across the facets, different lasing threshold currents are observed across different channels of WBL. The lasing threshold also varies depending on from which WBL facet the spectrum is collected.

Table 7 SOA number, facet number, lasing current threshold

SOA number	2	3	4	5	6	8	9	10	11	12
Facet number	f3	f5	f7	f9	f11	f15	f17	f19	f4	f2
Lasing current (mA) (Input)	28	40	80	80	40	NA	75	70	45	50
Facet number	f22	f20	f18	f16	f14	f10	f8	f6	f14	f23
Lasing current (mA) (output)	28	40	80	80	40	80	80	80	65	55

3.2.3 Insertion loss measurement

WBL channels controlled by SOAs 2,3,4,5,6,9,10,11,12 were further characterized by injecting laser light into the wavelength channels, while the SOAs are tuned at 40 mA of current. The end-to-end insertion losses are plotted in Figure 14. Channels corresponding to SOA 2,3 and 6 have end-to-end insertion losses of 32 dB, 32.8 dB and 34.6 dBs, respectively while the other channels have end-to-end insertion losses exceeding 40 dB. The hybrid coupling losses per SiPh/InP facet were then estimated by considering fiber-to-SiPh chip coupling loss, any excess loss in the fibers and gains of the SOA. Considering 3 dB/facet fiber-to-chip coupling losses, and 5 dB of the SOA gain, the hybrid minimum and maximum coupling loss corresponds to 13.5 dB/facet for Ch2 and 24 dB for channel 12 respectively, all the other channel loss/ facet are listed in Table.8.

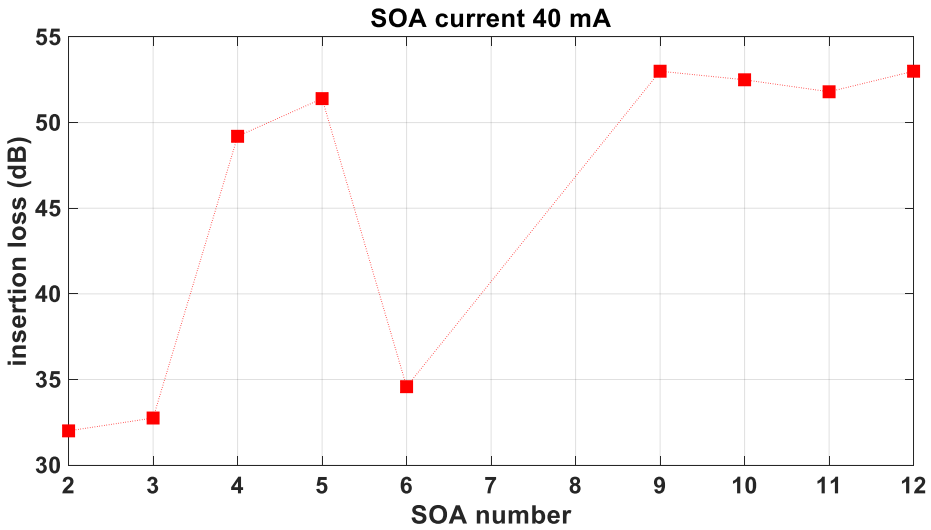

Figure 14. End-to-end insertion loss measurement hybrid WBL channels

Table 8 Insertion loss measurement of the wavelength channels

SOA number	2	3	4	5	6	9	10	11	12
Facet #	[f3, f22]	[f5, f20]	[f7, f18]	[f9, f16]	[f11, f14]	[f17, f8]	[f19, f6]	[f4, f14]	[f2, f23]
Channel #	10	8	6	4	2	5	7	9	11
End-to-end insertion loss (dB)	32	32.8	49.2	51.4	34.6	53	52.5	51.8	53
Hybrid coupling loss/facet (dB) *	13.5	13.9	22.1	23.2	14.8	24	23.75	23.4	24

(*) calibrated with 3 dB/facet coupling loss, 4 dB excess loss in the fiber, 5 dB SOA gain @40mA)

4 CONCLUSIONS

The presented solutions represent a technological advancement in HL4 node level switching design based on WBL. Here AWGs with 100 GHz granularity have been integrated in the hybrid PIC. Moreover, 50 GHz granularity obtained by reliable AWGs design integrated on a SiPh PIC have been already demonstrated, allowing for even more dense WDM spacings. Due to the particular relevance and complexity the main objective of this deliverable has been to perform the characterization of the WBL structure which includes both SOAs and wavelength multiplexing structures, while MCSs are less relevant as present a simpler hybrid integrated architecture [4].

The preliminary results on the characterization of the first 2 assembled WBL chips demonstrated the effectiveness of the performed F/C bonding, although some refinement needs to be applied. Moreover, a careful management of the A/R coated SOAs and a more accurate flip-chip alignment into SOI cavities will be developed to maximize the switching and gain characteristics of SOAs and overcome the extra losses.

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6 ACRONYMS

AR	Antireflection
AWG	Arrayed Waveguide Grating
DeMux/Mux	de-multiplexing/multiplexing
E/O	electro/optical
F/C	Flip chip
FSR	Free Spectral Range
HLn	Hierarchy Level n
InP	Indium Phosphide
I-V	Current-voltage
MCS	Multicast switch
MFD	Mode field diameter
PIC	Photonics Integrated Chip
Si Ph	Silicon Photonics
Sn	Tin
SOA	Semiconductor Optical Amplifier
SOI	Silicon On Insulator
WBL	Wavelength blocker
WDM	Wavelength-Division Multiplexing
WSS	Wavelength Selective Switch