D4.4 SiPh circuitry for hybrid integrated low insertion loss MCS

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Disclaimer

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EXECUTIVE SUMMARY

PASSION introduces new photonic technologies and devices for supporting agile metro networks, capable of enabling target capacities of Tb/s per channel, 100 Tb/s per link and Pb/s per node over increased transport distances in the range of few hundreds of kilometers. The modularity and programmability (via Software Defined Networking: SDN) of the system components of the node is used to achieve the flexibility and agility level demanded by the dynamic traffic, channel bandwidth/path/state/energy requirements of the metro network.

The PASSION switching nodes are designed to function as a reconfigurable add and drop multiplexer (ROADM) within metro network. The drop part of the node diverts some of the link traffic to drop it at the receiver side. The multicast switch (MCS) adopts a broadcast-and-select scheme. That means an input signal of the MCS is broadcasted by a splitter to all output ports and is selected by a dedicated space switch at the output port. These functionalities are greatly helpful to add re-configurablity and to efficiently use the available receiver modules. However, as the number of output ports of MCS increases, the insertion loss increases due to the splitter within MCS. Compensating these losses requires deployment of high cost EDFA thereby limiting scalablity. Therefore, the implementation of small-footprint and low-insertion loss MCS for a node featuring traffic aggregation/disaggregation is an important criteria.

This deliverable document reports the design of SiPh circuitry for hybrid integrated low insertion loss MCS in the drop data path. Low insertion loss implementation of the MCS is enabled by combining three design aspects. The first one is the incorporation of booster SOA amplifiers to compensate on-chip MCS insertion losses, which enables the scaling the number of ports. The second aspect is the low-loss SiPh circuitry which is used for the realization of hybrid integrated MCS. The third aspect is the low insertion losses achieved through high precision hybrid integration technology of SiPh passive and InP active circuitries with target coupling loss of less than 2 dB/facet.

The SiPh circuitry embeds functionalities such as *splitting*, *distributing (shuffling)*, and *space switching* to enable the *broadcast and select* feature within the MCS. The *spectral slicing* feature allows to limit the number of wavelengths going into an SOA-based MCS to avoid output power saturation. The *spectral slicing* is enabled via a 2-stage Mach-Zehnder Interferometric (MZI) 1x4 de-multiplexer. The *space switching* is enabled by a hybrid integration of low-loss SiPh passives (power combiners) and InP SOA array switching gates. The low insertion loss within the SiPh circuitry will be used to realize energy-efficient MCS. Scalability of the switches to high channel count/capacity is done by following a modular approach in a pay-as-you-grow manner while integrated SOAs are used to compensate the incurred losses. The presented low loss hybrid integrated MCS design is instrumental towards building compact and energy efficient circuitries for metro switching nodes.

1 INTRODUCTION

1.1 BACKGROUND AND MOTIVATION

The PASSION project works towards the development of application driven photonic technologies supporting innovative transceivers and optical nodes featuring different levels of aggregation (in spectrum, and space) for an envisaged network architecture (shown in Fig.1) which is able to match the growing traffic demand in the metro connections. The PASSION approach is capable of establishing high capacity connection for metro network distances (typical few hundreds of km) with high throughput, low-cost, energy-efficient and reduced footprint devices for massive deployment. End-to-end connectivity for novel services and businesses is achieved with dynamic SDN control of the different systems and subsystems to ensure metro connectivity and deployment of services. With the introduction of new modular photonic technology devices, PASSION is capable to reach capacity of Tb/s per channel, 100 Tb/s per link and Pb/s per node.

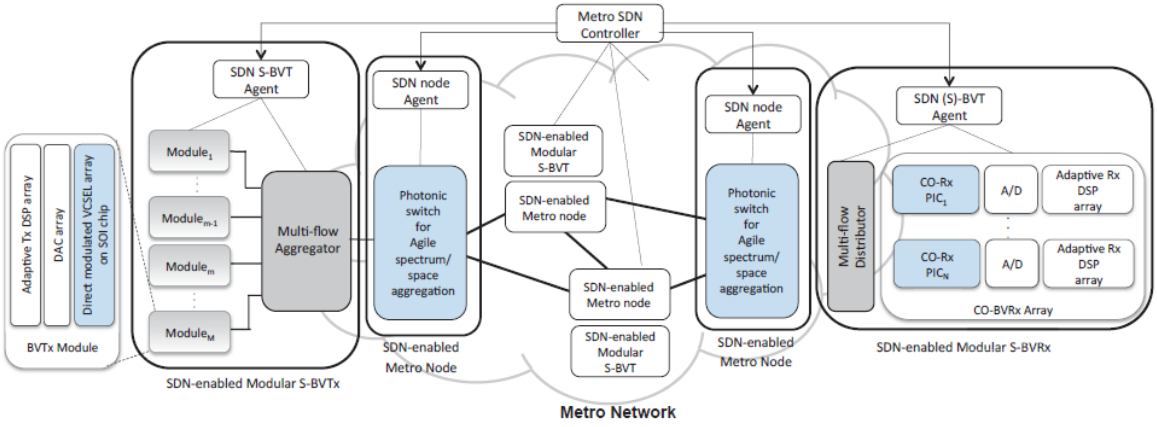


Figure 1 PASSION metro network: envisioned infrastructure, supported by new device technology developments

The growth of internet traffic and particularly bandwidth intensive application such as video, coupled with dynamic and mobile data sources are the driving wheels behind the demand for provisioning of transparent and agile metro networks [1]. To effectively utilize the available spectrum and to allow compatibility with the pre-existing transmission systems, it is very essential to develop a node that can efficiently handle dynamic and growing traffic conditions. Furthermore, it is essential that the nodes are equipped with energy-efficient and small-footprint switching technologies given the increasing energy demands of global telecommunications infrastructure [2 - 4].

Current state of the art metro networks are quite static and present limited flexibility and scalability. The metro network architecture within PASSION project will be a key enabler of network flexibility and agility required to address cost and efficiency requirements. Increased system flexibility is adopted with sliceable bandwidth/bitrate variable transmitters (S-BVTs) combined with a node featuring traffic aggregation/disaggregation together with switching in space and wavelength. Increase in the capacity is handled with agile aggregation in the spectrum, polarization and space dimensions. This metro network concept will leverage modularity and exploits the SDN (software defined networking) paradigm inorder to efficiently allocate/use the overall network resources transforming the operation of today's network infrastructure and reducing overprovisioning and margins.

Fig. 2 shows the architecture of an optical switching node in the PASSION project. It consists of optical switching components for handling *express traffic*, *added traffic* and *dropped traffic*. The express traffic is carried by multi-core fibers (MCF) or fiber bundles, where SMF is used to connect the MCF with optical switching node via Fan out/ Fan in structures. The *S-BVT*s are used to transmit the locally generated traffic with variable bandwidth/bitrate at that particular node. Both the generated traffic and aggregated traffic are merged as *added traffic*. The switching functionality is implemented via *photonic switching module (PSM)*, *Add switches*, *Aggregate/disaggregate switches*, and *Multicast switches (MCS).* The *PSM* provides higher level connectivity by switching the traffic at any input port to any output port which are either assigned to *express out* path or *dropped traffic* path. The *Add switch* provides WDM switching, merging and aggregating tasks for the locally generated traffic. The *Agg/disaggregate* switches are WDM enabled interleaving between the dropped traffic and aggregated traffic.

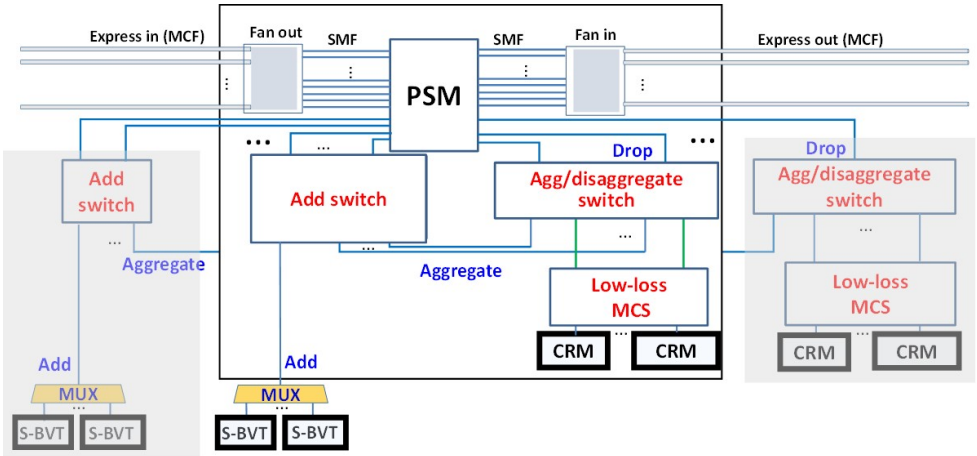


Figure 2 PASSION switching node, modular design, Low loss Multi-cast switch node (drop)

The Aggregation/disaggregate functionality maximizes resource utilization by bundling traffic of same destination in a single MCF, which are forwarded as bypass traffic in express path before reaching the destination node. The implementation of these switching functionalities makes use of the combination of Wavelength Selective Switches (WSS) and Space Switches. In the optical switching node, the drop part is augmented by an aggressive on-chip design, where fully meshed connectivity and channel selectivity is provided to connect with the available coherent receiver modules (CRM). This brings to large-scale integration and circuitry choices for the multi-cast switch (MCS) which has a broadcast-and-select functionality. The number of dropped wavelengths is equal to the number of output ports of the MCS. If it is desired to increase the number of dropped wavelengths, it is necessary to increase the number of output ports of the MCS. One of the limitations experienced in scaling the MCS is the inherent insertion loss of the broadcasting splitter that scales with number of output ports.

Therefore, low insertion is an important design metric of the MCS allowing to scale the number of ports. This is approached from three aspects. First, by incorporating on-chip amplification within the MCS design, the insertion loss is minimized. Second, by using low-loss SiPh circuitry, the insertion loss of the MCS is minimized. Third, the design for high-precision hybrid integration insures low fiber-to-chip coupling losses of the MCS circuit. This deliverable report discusses the design of low-insertion loss SiPh passives for the realization of hybrid integrated MCS.

1.2 TARGET OBJECTIVES

For the realization of low insertion loss hybrid MCS, circuit design SiPh and InP platforms will be executed in parallel, in order to push chip compactness and reduce insertion loss. Aggressive optical loss reduction is sought through hybrid integration of passives on SiPh with InP active elements. The *broadcast-and-select* MCS functionality is implemented via hybrid integration of SOA switching gates and low loss SiPh circuitries (power splitter/combiner and shuffle networks). Hence, the following strategies will be adopted for the realization and demonstration of the low-loss hybrid MCS.

1. SiPh chip consisting of low loss circuitries for spectral slicing and broadcasting is designed and will be fabricated on VTT's platform.
2. InP chip consisting of SOA arrays to be used as switching gates of the space switch is designed and is currently being fabricated.
3. Finally, assembly processes for low loss hybrid integrated MCS will be done in the premises of VTT.

2 MULTI-CAST SWITCHES (MCS)

An optical multicast switch provides cost-effective solution to realize a colorless, directionless, and contentionless functionality to enhance the operability in a multi-degree ROADM. Fig. 3 shows a typical architecture of an MCS, with *M* input ports and *N* output ports.

With its *broadcast-and-select* scheme, the MCS will be able to transfer as many as *N* wavelengths to the attached receiver modules from *M* directions. At each of the inputs of the MCS, a *1xN* splitter broadcasts the input signal to all output ports. An *NM x NM* shuffle network is used to distribute the copies of all inputs signals to all output ports.

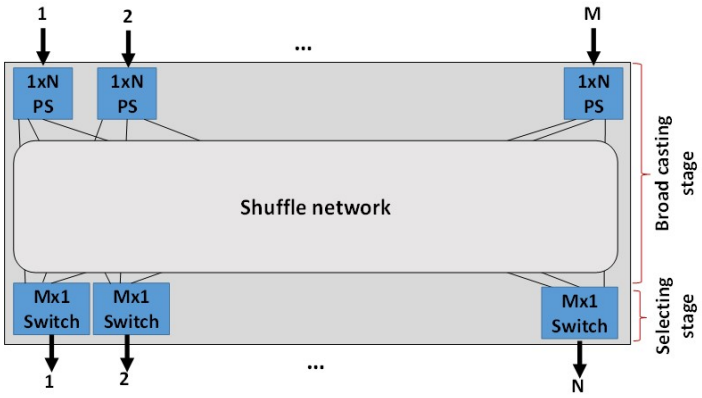


Figure 3 Schematic of a multi-cast switch (MCS)

At each of the outputs of the MCS a space switch is used to select the signal from one of the inputs. Due to the fact that each *M×1* switch can select any direction (therefore achieving the "directionless" function) and only one at a time, it is not possible for two or more signals of the same wavelength from two or more directions to collide with each other, thereby achieving the "contention less" function. Furthermore, the MCS is "colorless" because there is no wavelength-dependent component in its structure. In combination with coherent-receivers, the desired wavelengths are selected by tuning a local oscillator (LO) laser without needing an extra optical wavelength filter.

It is to be noted that the number of wavelengths that can be dropped simultaneously is equivalent to the number of output ports of the MCS. If it is desired to increase the number of output ports *N*, the insertion loss of the *1xN* power splitter (PS) increases, requiring high cost EDFA to compensate splitter losses and thereby increasing deployment costs. Therefore, it is important to incorporate low-cost amplifier components within the MCS design to support scalability.

2.1 LOW LOSS MCS : THE PASSION APPROACH

Due to the inherent loss of splitters within the MCS, it is unavoidable to make use of amplifiers to compensate the losses and support scalability. In the PASSION approach, we implement a photonic integrated circuit (PIC) MCS design with a low-cost amplification based on SOAs, thereby avoiding the need for high cost EDFA. Fig. 4 shows the schematic representation of on-chip MCS design with *M* inputs and *N* output ports.

At each of the *M* input ports an SOA boosts the input signal to compensate the fiber-to-chip coupling losses and *1xN* PS insertion losses. Then, a 1x*N* PS broadcasts the input signal to all output ports.

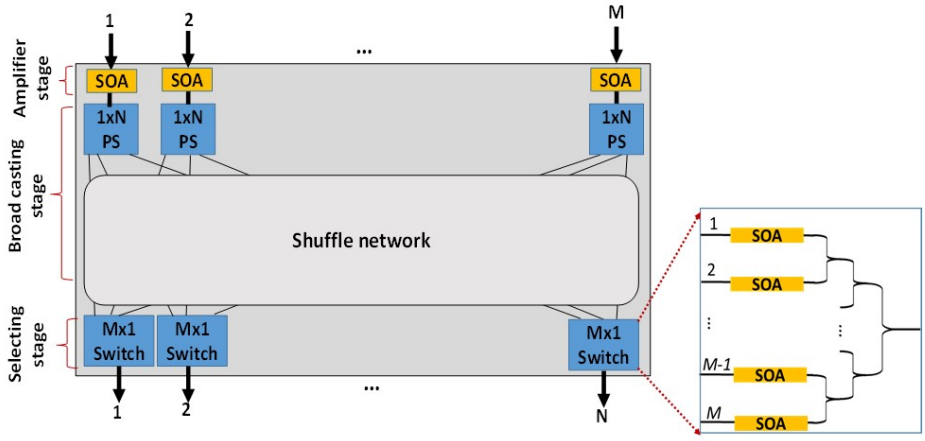


Figure 4 Schematic of on chip MCS design

Then a *NM* x *NM* shuffle network is used to distribute the copies of the signal from *M* input ports to *N* output ports. At each of the *N* output ports, an *Mx1* space switch is used to select one of the signal from one of the *M* input ports. It can be seen that the *Mx1* space switch is implemented by an array of *M* SOA gates and *Mx1* power combiner as can be seen in Fig. 4. The SOA gates can be turned *On/Off* to either select or suppress the signals broadcasted from one of the *M* input ports. With this architecture, the on-chip MCS design allows CDC operation while allowing the efficient use of resources of the attached CRM modules. This presented design will be implemented into two target platforms namely the SOAs array design to be implemented on InP and the passive circuitry of the MCS in low-loss SiPh platform. Then, the MCS will be implemented following a hybrid integration scheme which will be described in section 3 and 4.

2.2 MODULAR DESIGN AND SCALABILITY

To support the growing capacity demands in the metro networks, it is expected that the switching node should adopt a scalable design. As discussed in the previous section, the number of dropped wavelengths is directly related to the number of output ports *N* of the MCS. That means, for a total number of input wavelengths at MCS, a single MCS module can drop only *N* number of wavelengths at a time. The high port count of the MCS demanded by the high capacity requirement poses a limitation on the number of ports that are practically realizable in a single PIC per MCS functionality.

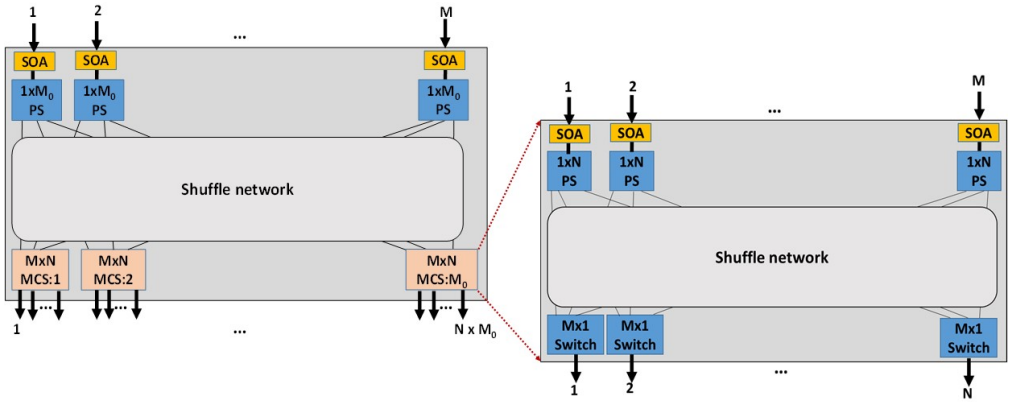


Figure 5 Modular implementation of multi-cast switch within PASSION switching node, M_0 modules of NxM MCS switch

Modular design of the MCS solves this. That means that by using M_o modules of the MCS, the number of dropped wavelengths can be increased to $N*M_o$. On the other hand, reduced switching flexibility is incurred (i.e. not being able to reach any output port from any input port). This can be solved by using a separate shuffling network for interconnectivity between the modules at a cost of slight increase in complexity.

A schematic of MCS containing M_0 number of *NxM* MCS modules, with *M* input ports and M_0*N output ports is shown in Fig. 5. Since the number of outputs is scaled to M_0*N, the number of dropped wavelengths is scaled to M_0*N. At each of the *M* input ports $1x\ M_0$, power splitter is used to broadcast the input signal to all MCS modules. The broadcasted signals are routed to each MCS via M_0*N x M_0*N shuffle network. This presented approach supports a high degree of connectivity, in that any wavelength injected in one of the *M* input ports can be dropped to any of M_0*N output ports.

Another aspect of the SOA based low-loss MCS design is ensuring that no distortion is introduced into the signal because of large input power injected into the high power SOAs. In order to reduce the input power, the number of wavelengths input into SOA is limited by using waveband de-multiplexing (spectral slicing), while the MCS functionality is duplicated for each output of the de-multiplexer. Then, the MCS functionality is then replicated for all outputs of de-multiplexer to ensure that any of the input signals of the MCS is not distorted. The MCS design based on this concept is given in sections 3.

3 HYBRID INTEGRATED LOW LOSS MULTI-CAST SWITCH

The low-loss hybrid integrated MCS implementation, within PASSION project makes use of InP actives (SOAs) and SiPh based on passives. The hybrid design has two fold advantages in realizing the low-loss MCS. The first advantage is the design of MCS consisting of splitters and shuffle network in low-loss SiPh platform. The second advantage is the realization of low fiber to chip coupling loss of MCS due to better mode field matching of 3 μm wide SiPh waveguide. The mask layout of passive circuitries on SiPh and active circutry on InP are designed to facilitate hybrid integration.

3.1 HYBRID INTEGRATION OF SIPH PASSIVES AND INP ACTIVES

Efficient optical coupling of InP to the SiPh waveguides via hybrid integration is dependent on alignment with precisions in the sub-µm range. Active alignment techniques prove to be time-consuming and expensive technique. Rather, passive alignment technique conducted by using high precision mechanical placement of the chip can generate optical packaging with a coupling loss lower than 2 dB/facet. Flip-chip bonding of InP chip onto SiPh can provide an efficient electrical interconnection via solder bumps to the InP chip and a bonding material on the substrate. Furthermore, unlike wire bonding, it provides high density and shorter electrical interconnection thus enables reduced die size and higher speed operation.

Therefore, for the hybrid integration of the MCS, a flip-chip bonding with a well-controlled passive opto-mechanical alignment technique developed by a partner institution VTT will be followed. A schematic of the intended flip-chip bonding process is shown in Fig. 6. In order to minimize the coupling loss, the waveguide modes of the two chips must be matched. For this, good control of the lateral and vertical off-set has to be assured to minimize the gap between the chips. A vertical alignment/positioning accuracy of less than ± 0.5 μm is required. It is possible to directly bond the InP chip and the SiPh together via a thermal compression (TC) technique [6]. In TC bonding, the Au-coated contact pads of the InP and SiPh chips are bonded together thanks to the combined effect of elevated temperature (typically >300°C) and bonding pressure. The good control in the thickness of the deposited thin films and the Silicon oxide stoppers then provides excellent vertical alignment [7]. The InP chip will be flipped down onto a SiPh cavity, where the solder bumps will be used for electrical bonding. The SiPh cavity is designed complimentary to the InP chip. The depth of the cavity is adjusted so that the optical axis of the InP waveguide core aligns with that of the SiPh waveguide after flip-chip bonding.

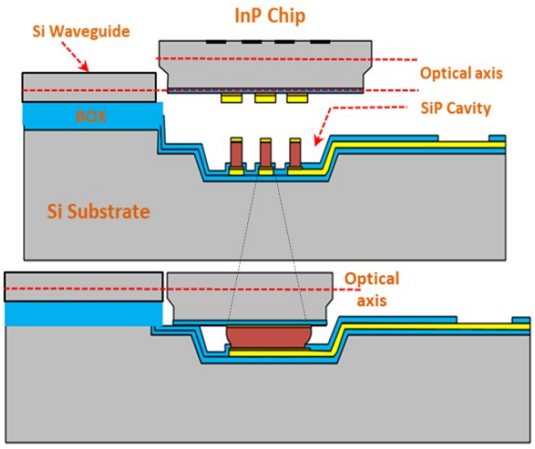


Figure 6 Schematic of the flip-chip bonding process

The cavity has vertical stoppers on three sides so that the waveguide cores are self-aligned during assembly. Alignment in the lateral direction is achieved with U-bend waveguide that start out as straight waveguide on the SiPh chip, continue into the InP chip where we design the U-bend, and exit back into the SiPh chip. Metal pads, correspondent to the ones on the InP chip, are defined at the bottom of the SiPh cavity and will be utilized for making electrical connections to the InP chip. Metal lines with a pitch of 250 μm run out of these metal pads, and are routed to the south edge of the SiPh chip for probing purposes. The details of the SiPh and InP circuitry design for low-loss MCS design is given in the next section.

3.2 CIRCUIT FUNCTIONALITIES

As discussed in Section 2, the low-loss implementation of MCS in the PASSION project, has the capability to scale the number of dropped wavelengths. In order to avoid the booster SOA output power saturation, the concept of spectrum slicing (waveband de-multiplexing) is introduced. An MCS switch design incorporating spectral slicing is shown in Fig. 7.

The number of wavelengths per input fibre is 40 according to modularity definition given in Deliverable 4.1. The spectral slicing is implemented by 1x4 Inter-leaver (de-multiplexer). 40 channels with 100 GHz spacing at the input port of the Inter-leaver are distributed to 10 channels with 400 GHz spacing at each output port of the Inter-leaver. In this way, the number of wavelengths going into the booster SOA is reduced from 40 to 10. After amplification, the 4 output ports of the Inter-leaver are broadcasted to all output ports of the MCS by a 1x8 PS and shuffle network. The number of broadcasted signal outputs is 32, therefore a 32 x 32 shuffle network is used.

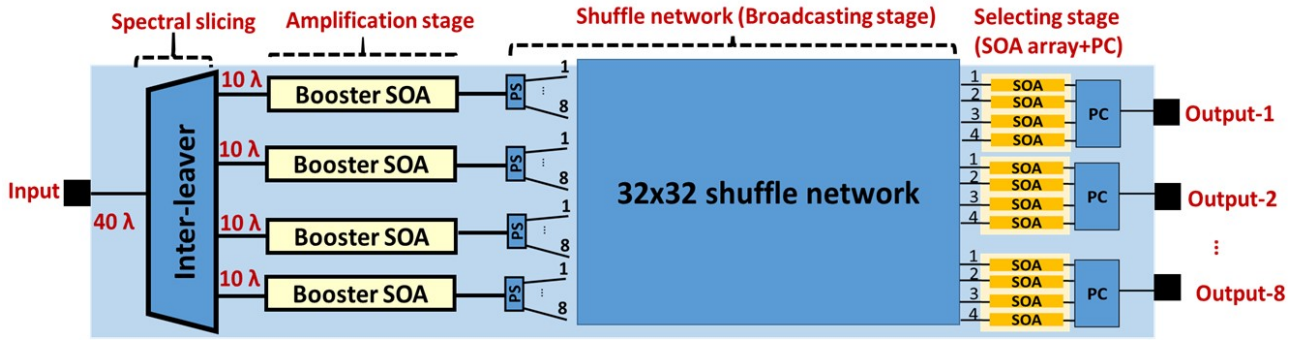


Figure 7 1x8 MCS with spectral amplification, slicing, and broadcasting

At each output of the MCS a 4x1 space switch is used to select one of the inputs distributed by the shuffle network. The 4x1 space switch is composed of 4 SOA gates connected to the 4:1 power combiner (PC).

In this section, we introduce the MCS circuit functionalities spectral slicing, boosting, broadcasting and space switching to be implemented in low-loss SiPh platform.

3.2.1 Spectral slicing (MZI – based Interleaver)

The concept of spectral slicing within the MCS design reduces the number of wavelengths going to a booster SOA from 40 to 10, so to avoid output power saturation. For this, a two stage 1x4 MZI based interleaver shown in Fig. 8 is designed.

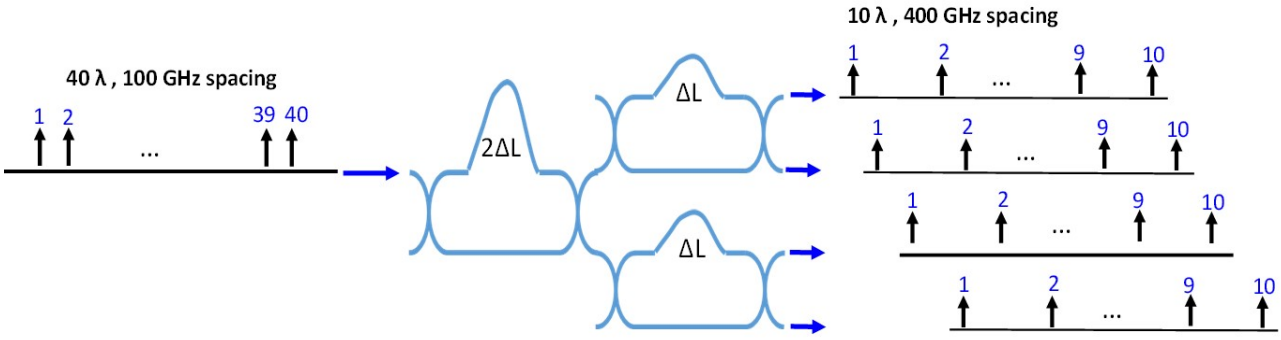
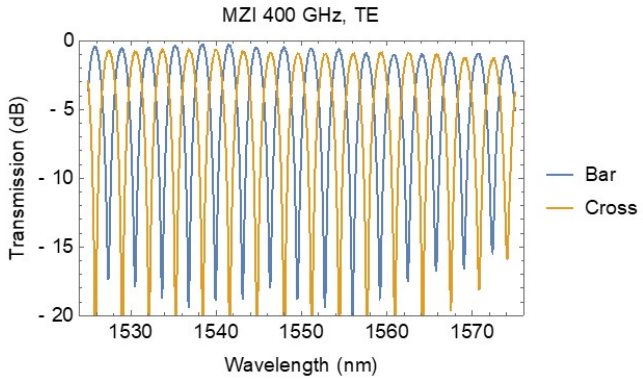
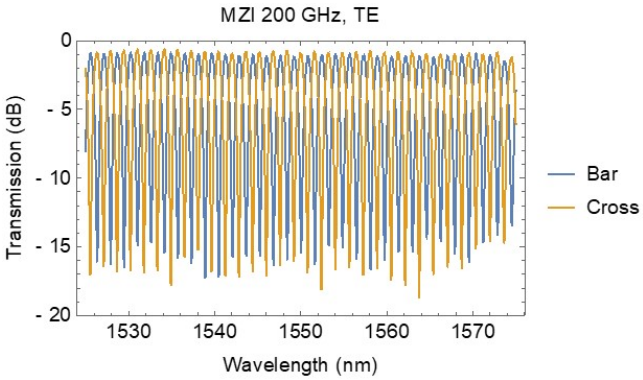


Figure 8 Schematic representation of a 1x4 MZI interleaver for (input from 100 GHz: 400 GHz) spacing

The length imbalance of the 1st and 2nd MZI stages corresponding to ΔL and 2 ΔL is used to transform the 100 GHz spaced channels into 400 GHz spaced channels. The 4 outputs of the interleaver are shifted by 100 GHz relative to each other.
The input signal has a 100 GHz channel spacing, therefore, the 1st stage MZI has a channel spacing of 100 GHz and FSR of 200 GHz. The second MZI stage has a channel spacing of 200 GHz and an FSR of 400 GHz. Therefore, the outputs signal has 400 GHz channel spacing and are shifted by 100 GHz relative to each other.



(a)



(b)

Figure 9 Characterization of MZI interleaver with a channel spacing of (a) 400 GHz (b) 200 GHz

This 100 GHz: 400 GHz Inter-leaver has already been designed, fabricated and tested at the partner institution VTT. The experimental characterization results are given in Fig. 9. Both the MZI designs for the 400 and 200 GHz FSR values have been individually characterized, and the measured transmission plots are presented in Fig. 9. Measurements show good results with low insertion loss (0.3-1.0 dB) in the region of interest, and reasonably good extinction ratio (15-20 dB). The Inter-leaver design is therefore instrumental to the realization of low-loss MCS.

3.2.2 Boosting (SOA amplification)

The boosting amplifier is based on SOAs and compensates the loss of the broadcasting part of the MCS. The SOAs are designed in InP platform in an SOA array chip. The SOA array chip contains both boosting (amplification) and gate switching functionality incorporated in the same InP chip. The schematic representation of this chip and the mask layout are shown in Fig.10 (a) and Fig. 10 (b) respectively. It is to be noted the input/ output of the InP chip is routed to the same side to facilitate hybrid integration.

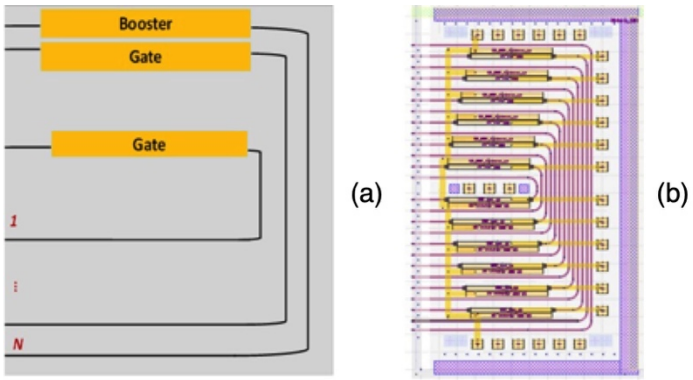


Figure 10 SOA array InP chip containing boosting and gate switches (a) schematic N SOA arrays (b) mask layout of 12 SOAs

3.2.3 Broadcasting (shuffle network)

The broadcasting functionality of the MCS consists of a number of splitters and shuffling network that distributes the copies of the input signal into a number of space switches. For the 1x8 MCS design represented in the schematic in Fig. 7, a 32 x 32 shuffle network is needed. In order to experimentally characterize the impact of waveguide crossing within a 1x8 MCS, a 32 x 32 shuffle network is designed. The schematic representation and its mask layout is given in Fig.11(a) and Fig. 11(b) respectively. This shuffle network consists of a 121 waveguide crossings. In the broadcast network of 1x8 MCS, a signal passes through minimum of 0 waveguide crossing and a maximum of 15 waveguide crossings.

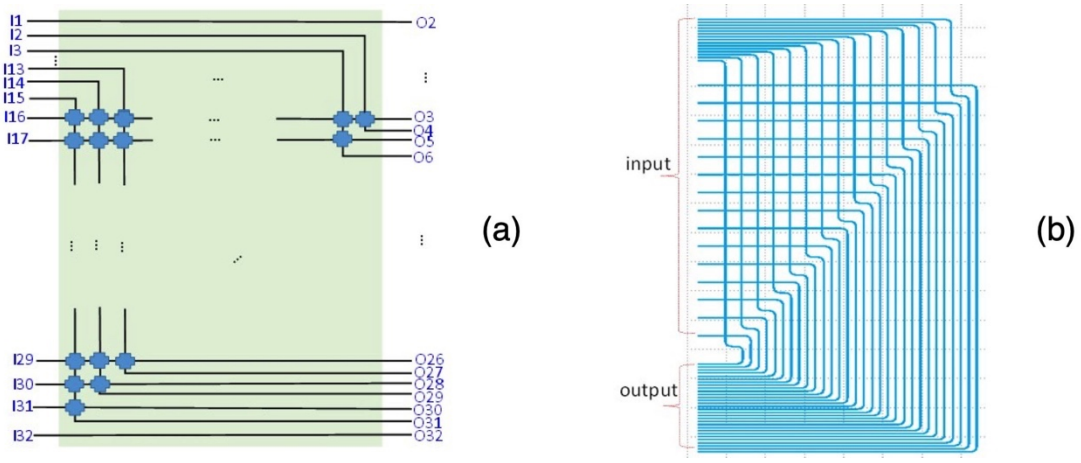


Figure 11 32 x32 shuffle network (a) Schematic representation (b) mask layout

3.2.4 Space switching (SOA gates)

The *M* x1 space switching functionality within the MCS is used to select one of the signals from one of the *M* input ports.The switching functionality is implemented with *M* SOA array switching gates, while the passive circuitry for the M:1 power combiner is implemented in low loss SiPh platform as can be seen in the schematic representation shown in Fig.12. The input to SOA array switch gates is coupled from the shufffle network in SiPh. It is to be noted that, for ease of hybrid integration, the SOA array input/output waveguides are put in one side. By turning *On* one of the SOAs the desired signal from one of the MCS input ports is selected. During *Off* state of the SOAs the input signals are suppressed. The output signals all *M* SOA switching gates are coupled to a *M*:1 power combiner SiPh, the output of which is routed to the output port of the MCS. The *M*:1 power combiner is designed by cascading 2:1 50:50 MMI couplers.

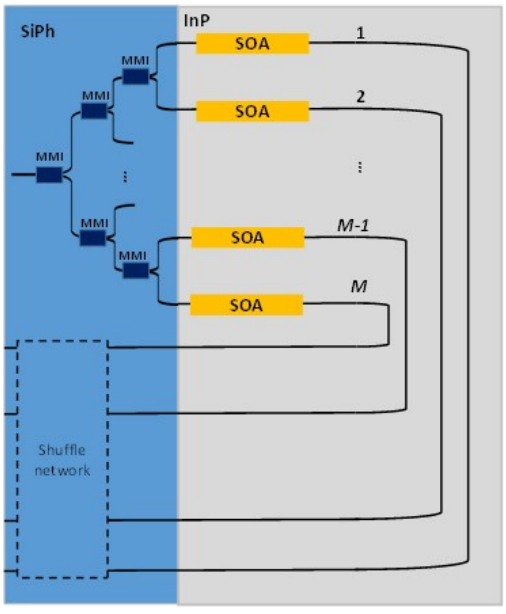


Figure 12 Schematic representation of a hybrid M:1 space switch

4 LOW LOSS SIPH CIRCUITRY FOR HYBRID INTEGRATED MCS

As discussed in the previous section, the MCS functionalities are realized in both low-loss SiPh passives with InP actives. In this section, we report the initial design activity of SiPh passives towards the realization of low-loss hybrid integrated MCS. The presented design is a 1x2 MCS, i.e. has one input port and two output ports. Therefore, two InP SOA array chips where each chip is used for both boosting (amplification), and gating (switching) are incorporated. Within, the SiPh photonic chip in addition to MCS circuitry, cavity designs are incorporated to accommodate the InP chip for flip-chip bonding during hybrid integration.

4.1 1X2 HYBRID INTEGRATED MCS

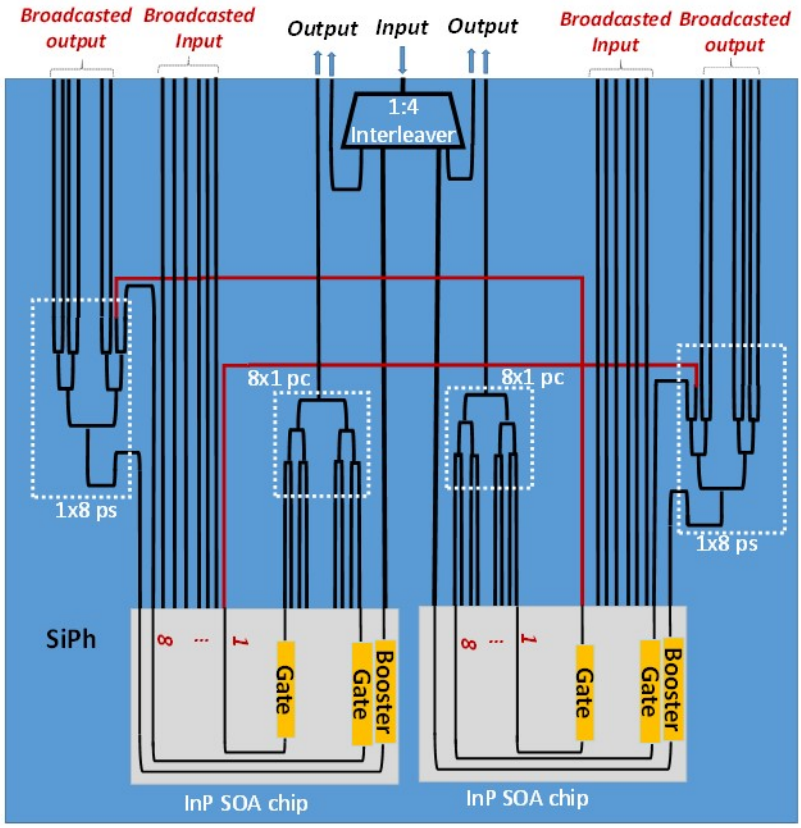


Figure 13 Low loss MCS design (to be realized after hybrid integration)

Figure.13 shows the schematic representation of a 1x2 hybrid integrated MCS, consisting of *spectral slicing*, *boosting* (amplification), *broadcast-and-select* functionalities. The impact of shuffle network containing waveguide crossings are introduced via test input ports (labelled as *broadcasted input* in Fig.13). The input signal passes through a 1x4 MZI based inter-leaver as discussed in Section 3.2.1. Two of the output ports of the Inter-leaver are routed back as output. The other two remaining ports of the Inter-leaver are routed straight to the InP chip and are coupled into the booster SOAs of the two InP chips. It is to be noted that the input/output waveguides of the InP SOA chip are situated in one side. The amplified input signal is then coupled back to the SiPh chip to a 1x8 PS. Six of the eight output ports of the PS are routed as *Broadcasted output* to the outside of the SiPh chip. Two

of the eight output ports of the PS are routed within the chip as inputs to the two 8 x 1 space switches. The first output waveguide of the 1x8 PS is routed immediately to the InP SOA gate chip which is part of the 8 x 1 space switch. The second output waveguide (highlighted in red color) introduces a number of waveguide crossing while distributing the copy of the signals to the respective space switch. As a result, the distributed input signal passes through a maximum of 11 waveguide crossing at the input of the SOA array chip (input of the space switch).

The 8x1 space switching functionality is enabled by 8 SOA switching gates and 8x1 power combiners. The first two inputs of the space switches are distributed from within the chip, while the other 6 input signals of the space switch are introduced from outside the chip. The outputs of the 8 SOA switching gates are then coupled back to 8x1 power combiner (PC) on SiPh chip. The output of the two PCs are routed outside the chip as two outputs of the MCS.

4.2 MASK LAYOUT

Therefore, in the context of this deliverable, InP chip design at Tu/e and SiPh cavity design at VTT has been carried out for the hybrid integration of low loss MCS switch via flip-chipping. Flip-chip bonding of InP chip onto SiPh provides an efficient electrical interconnection system via solder bumps of the chip. Passive alignment technique conducted by using high precision mechanical placement of the chip can generate optical packaging with a coupling loss less than 2 dB/facet. The mask layout of the SiPh circuitry is designed to match the waveguide pitch with that of the InP SOA array chip. The SiPh circuitry occupies a footprint of 20 mm x 10 mm, while each InP chip occupies a size of 4 mmx 2.3 mm. Therefore, two cavities are designed in SiPh for placing the InP chip as shown in Fig. 14.

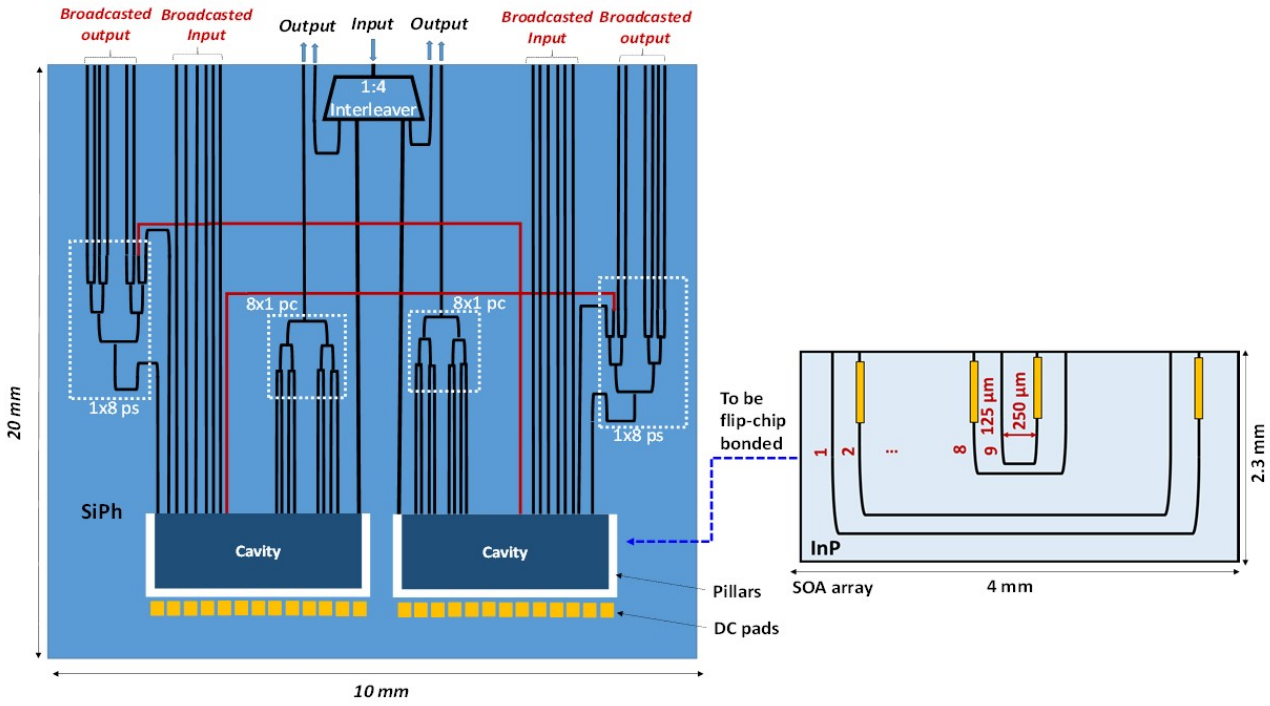


Figure 14 Schematic for low loss MCS: SiPh circutry, cavity and InP chip(to be realized after hybrid integration)

The cavity has the same size as that of the InP SOA array chip. Metal pads, complimentary to the ones on the InP chip, are defined at the bottom of the SiPh cavity. They will be utilized during the flip-chip bonding, and also for making electrical connections to the InP chip. Metal lines with a pitch of 250 μm run out of these metal pads, and are located at the bottom of the SiPh chip.

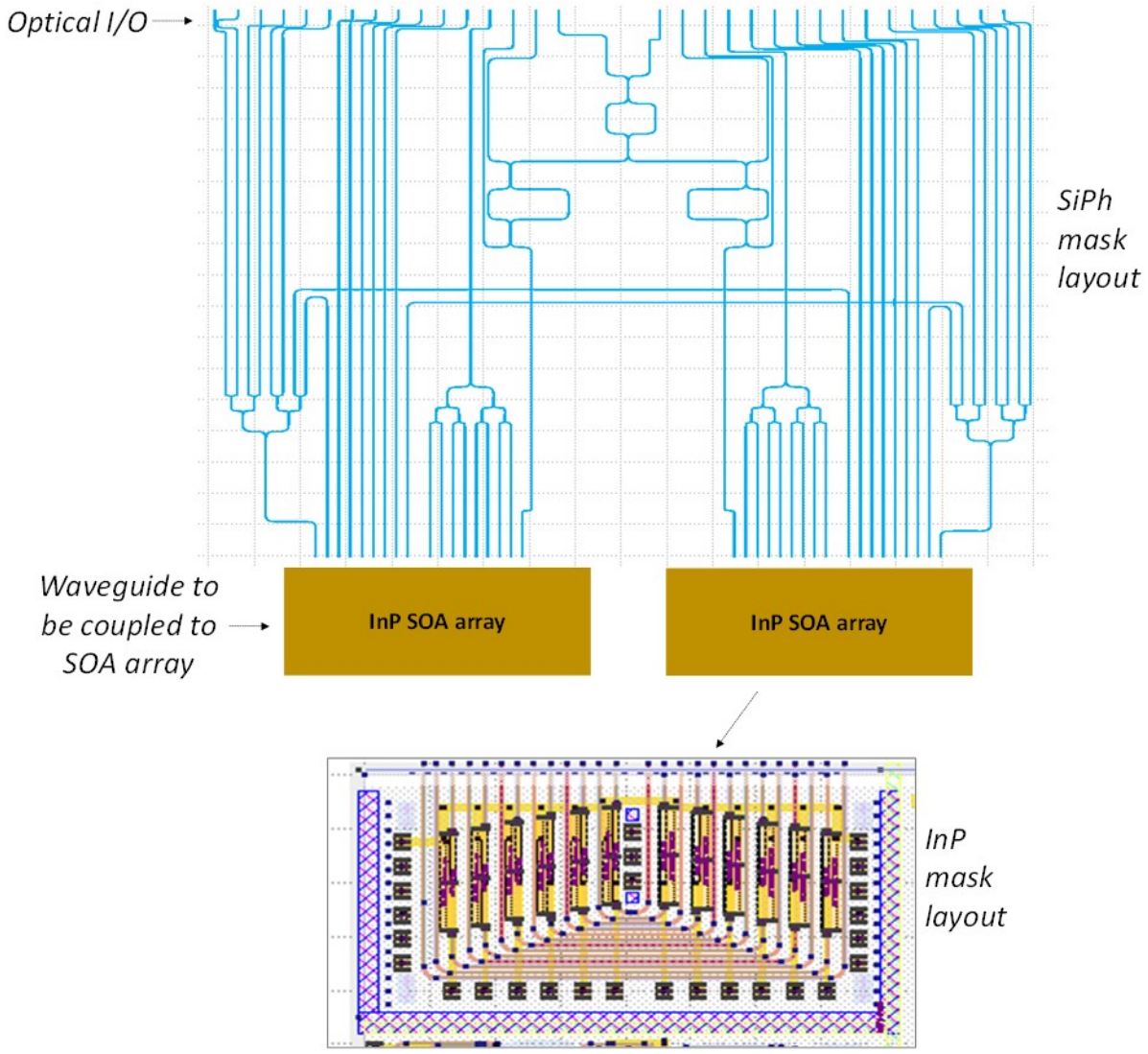


Figure 15 Mask layout of SiPh circuitry and InP SOA array chips to be used for 1x2 hybrid MCS

The cavity has pillars around the three edges excluding the side containing the waveguide input/output facet. The pillars serve as mechanical stoppers to be used to vertically position/align the core of the InP waveguide to that of the waveguide core in SiPh. After flip-chip bonding, the electrical contacts are routed to the top layer of SiPh and are found at the bottom edge of the chip for wirebonding with the external power supply. In order to minimize the risk of thermal cross-talk of the SOA array chip with the SiPh circuitry, the cavity is placed close to the south edge of the chip.

Fig. 15 shows the mask layout of the SiPh circuitry and InP SOA array chips for the implementation of the 1x2 hybrid MCS described in section 4.1. In the north edge of the chip the optical I/O are placed. A set of waveguides are placed with a pitch of 200 μm to be compatible with single mode

fiber (SMF) standard fiber array. In the southern edge of the chip the waveguides are routed to the two SiPh cavities for placing the InP SOA array chip.

After the fabrication of the SiPh and InP chips, flip-chip bonding with a well controlled passive opto-mechanical alignment technique developed by a partner institution VTT will be followed as discussed in section 3.1.

5 CONCLUSIONS

In this deliverable, the design of low-loss SiPh circuitry for realization of hybrid integrated multicast switch is reported. The hybrid MCS implementation makes of use of SiPh passive circuitry and InP active SOA array switches. The SiPh circuitry embeds functionalities such as spectral slicing, and space switching to enable the broadcast and select capability within the MCS. The spectral slicing implementation is enabled by a 2-stage Mach-Zehnder interferometric 1x4 de-multiplexer. The space switching is enabled by a hybrid integration of low-loss SiPh passives (splitters/combiners and shuffle network) and InP SOA array switching gates.

The low insertion loss within the SiPh circuitry will be used to realize energy-efficient MCS. The low loss implementation is tackled from three aspects: the first being the incorporation of boosting (amplifier) within the MCS circuit that compensates the splitting loss inherent within the MCS circuitry. The second aspect is the low-loss SiPh circuitry design involving high degree connectivity involving shuffle networks, power splitter and combiners. The third aspect is the hybrid integration of InP actives with SiPh passives. This is realized via passive alignment technique conducted by using high precision mechanical placement of the chip can generate optical packaging with a coupling loss less than 2 dB/facet. Flip-chip bonding of InP chip onto SiPh provides an efficient electrical interconnection system via solder bumps structure on the chip and a bonding material on the substrate.

The scalability to high number of ports is tackled by employing the principle of modularity in a pay-as-you-grow manner. The presented low loss MCS design targets energy efficiency within the PASSION switching node capable of supporting the requirements of current metro networks.

6 REFERENCES

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7 ACRONYMS

CRM	Coherent receiver modules
InP	Indium phosphide
MCF	Multi-core fibre
MCS	Multi-cast switch
MZI	Mach-Zehnder interferometer
LO	Local oscillator
PIC	Photonic integrated chips
PC	Power combiner
PS	Power splitter
PSM	Photonic switching module
S-BVT	Slicable bandwidth variable transmitter
SDN	Software defined network
SMF	Single mode fibre
SiPh	Silicon Photonics
SOA	Semiconductor optical amplifier
TC	Thermal compression
WDM	Wavelength division multiplexing
WSS	Wavelength selective switch