Intermediate report on the development of directly modulated VCSELs

Deliverable subtitle

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EXECUTIVE SUMMARY

The PASSION technology is based on sub-modules consisting of 40 DWDM C-Band vertical cavity surface emitting lasers (VCSELs) integrated on a single SiP chip. The 40 DWDM VCSELs cover a wavelength range from ITU channel 19 to 59, i.e from 1562.23 nm to 1530,33 nm. Each channel has a wavelength grid of 400 GHz (3.2 nm). These VCSELs will be directly modulated with discrete multitone (DMT) to achieve a transmission rate of 50 Gbps. For the development of the VCSELs required, a number of key developments and target parameters need to be met. As part of the design and manufacturing of VCSEL chips, Vertilas is evaluating reliability of the lasers in conjunction with the impact of exposing the lasers to bias current, heat and moisture. In addition, the lasers need to go through a burn-in procedure, followed by comprehensive characterisation of the static and dynamic chip parameters. To enable the evaluation within a lab set-up with further components, a high data rate RF package design is being developed.

VCSELs to cover such a wide wavelength span of 32 nm cannot be manufactured on a single wafer. Several wafers with specific wavelength parameters have to be designed and manufactured. This includes also special techniques to control the target wavelength of the wafers, as even the most advanced and state-of-the art epitaxy growth equipment features a certain material growth tolerance. The wavelength variation across one wafer needs to be controlled as well. Vertilas has developed techniques to control the wavelength both on 3” and 2” epitaxy equipment, including applying complex measurement equipment and procedures. In a first wafer run, Vertilas manufactured a 3” wafer and was able to meet the target wavelength with an accuracy of around 2-3 nm.

Furthermore, the VCSEL performance needs to meet the requirements of the PASSION application. The lasers should minimize electrical power consumption, optimize the modulation 3 dB bandwidth to around 20 GHz and provide sufficient optical power of around 3.5 mW. All VCSELs need to feature excellent single mode behaviour and the wafer yield needs to be high to provide a sufficient number of lasers. The VCSEL design has been adapted to these needs. A range of design optimizations have been applied to the VCSEL structure and corresponding production steps. The MQW active region has been modified, the resonator length and semiconductor mesa design reviewed to balance the above-mentioned requirements, such as optical power, side mode suppression ratio (SMSR), threshold current and other parameters. The basic VCSEL design requires a complex set of production steps, in particular due to the deployment of BCB (Bisbenzocyclotene) etching process to reduce intrinsic parasitic of the semiconductor material.

The first wafer run produced single mode lasers meeting the right wavelength around 1550 nm with an SMSR higher than 35 dB.

The lasers show some limitations, as a new processing step caused some problems during wafer production. Characterisation of the new wafer is still in progress and further data will be available in the coming 2-3 months. The issues are being fixed and next wafer runs are planned to be completed in the near future.

A large number of VCSEL samples have been supplied to project partners to support the integration efforts and system evaluation. VCSEL dies have been mounted and wire bonded on an evaluation board of the VCSEL driver.

1 VCSEL DESIGN

1.1 VCSEL STRUCTURE AND DESIGN

The VCSEL structure is based on a so-called short cavity (SC) buried tunnel junction (BTJ) VCSEL concept. In order to minimize the photon lifetime, the VCSEL consists of a very thin semiconductor structure including the active region and the BTJ. The top and bottom mirrors consist of dielectric materials instead of epitaxial grown mirrors.

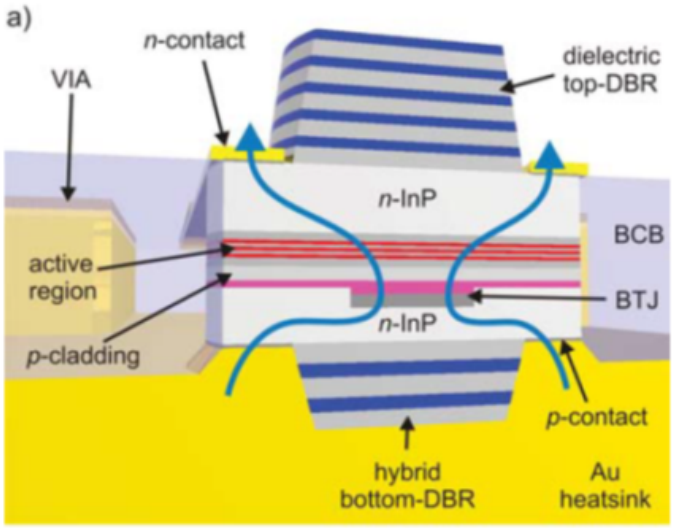

Figure 1. Cross section of short cavity InP BTJ VCSEL.

As part of the development efforts, the multiple quantum well (MQW) active region has been redesigned to optimize the structure of the quantum wells and barriers, incl. the strain. The buried tunnel junction and other layers have been verified for an optimal doping and thickness, including an evaluation of the tolerance of specific production steps.

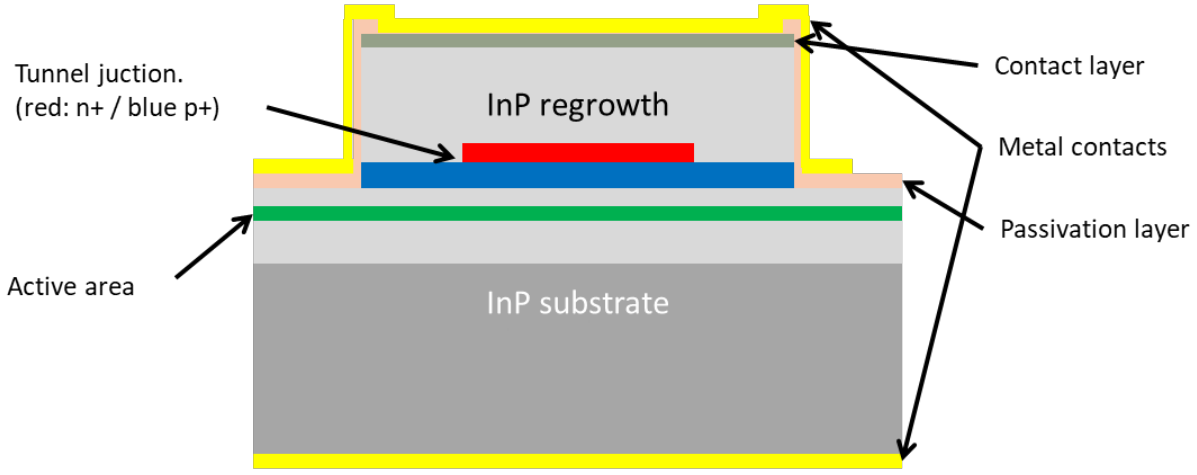

Figure 2. BTJ Test structure.

During the processing steps, the epitaxial material is being reduced by means of dry etching a mesa structure, to minimize the intrinsic parasitic. The void area after the mesa etching is filled with BCB.

Dielectric layers are being deposited above and below the BCB. Test structures have been manufactured and evaluated by means of focused ion beam (FIB), as shown in Fig. 3.

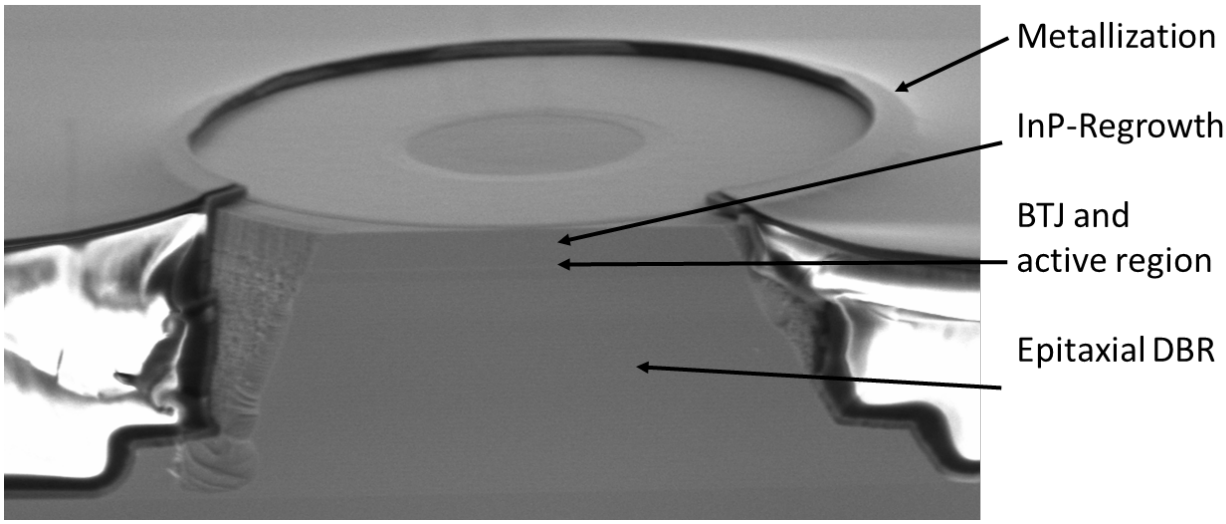

Figure 3. VCSEL test structure semiconductor mesa with BCB.

As results of these development efforts, a number of smaller and more significant changes have been applied to the shorty cavity VCSEL design. A new mask set has been generated and produced.

After discussion with project partners and assembly tests, the following VCSEL (Fig. 4) layout is suitable for flip chip integration and will be applied to the first wafer(s).

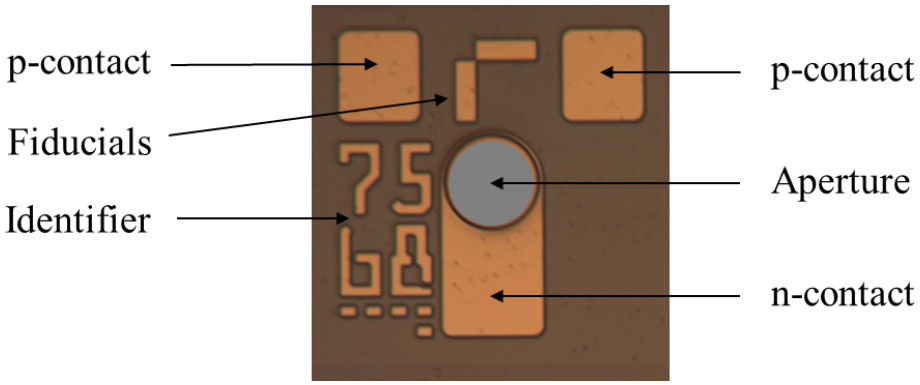

Figure 4.VCSEL Layout InP VCSEL.

Based on the results of the assembly and integration efforts, this VCSEL layout will be reviewed and may be optimized in the future.

1.2 VCSEL EPITAXY

For PASSION, the VCSELs should cover 40 ITU channels, this requires to develop and manufacture VCSELs from 1530 nm to 1562 nm.

As part of PASSION, epitaxy growth is being optimized for both 2” and 3” wafer equipment. The 3” epitaxy equipment has the benefit of a smaller inhomogeneity of the central wafer, compared with a 2” molecular-beam epitaxy (MBE). In addition, around double the number of VCSELs can be produced on a 3” wafer.

During the course of the project, it is planned to produce both 2” and 3” wafers.

Previous short cavity wafers showed quite a wide tolerance (+-15 nm) of the effective laser wavelength during the production steps. In order to optimize the VCSEL performance and meet the target wavelength(s), methodologies have been developed and optimized to implement an effective wavelength control of these production steps.

Various versions for the active region have been evaluated to optimize the performance. As mentioned in 1.1, semiconductor layers for the tunnel junction and regrowth are also performed as part of the epitaxy process.

1.3 VCSEL Processing

A cross section of the VCSEL is shown in Fig. 1 in Section 1.1. Processing of the top layers including the dielectric mirror requires quite complex production steps. After the mesa etching, BCB spin-on and curing steps, dielectric bottom mirror deposition and contact layer processing, a thick layer of plated gold is galvanized at the bottom of the wafer. In the following step, the original Indium Phosphide (InP) substrate is being etched down to the initial layers grown in the MBE.

Afterwards, the dielectric bottom mirror and metal contact processing is being performed. It is critical to apply some kind of coating around the dielectric mirror to protect it from moisture and potentially damaging exposure to other gases or materials. As mentioned before, one production step had an issue resulting in a limited performance of the VCSELs. Subsequently, a number of analysis and root cause steps were done. The next wafers are planned to be completed in the coming 2 to 3 months.

1.4 VCSEL Wafer Testing and Characterisation

Wafer testing and VCSEL characterization are performed by several steps:

- Wafer probing (P-I-V curves, SMSR)
- Wafer dicing
- VCSEL mounting on carriers and TO packages for testing of static and dynamic parameters

Due to an issue with one processing step, the performance of the VCSELs on this wafer is limited. The SMSR is > 35dB (Fig. 5), the max. optical power is around 2.5 mW (Fig. 6) and the threshold current is around 2 mA. Detailed characterization and further tests are in progress.

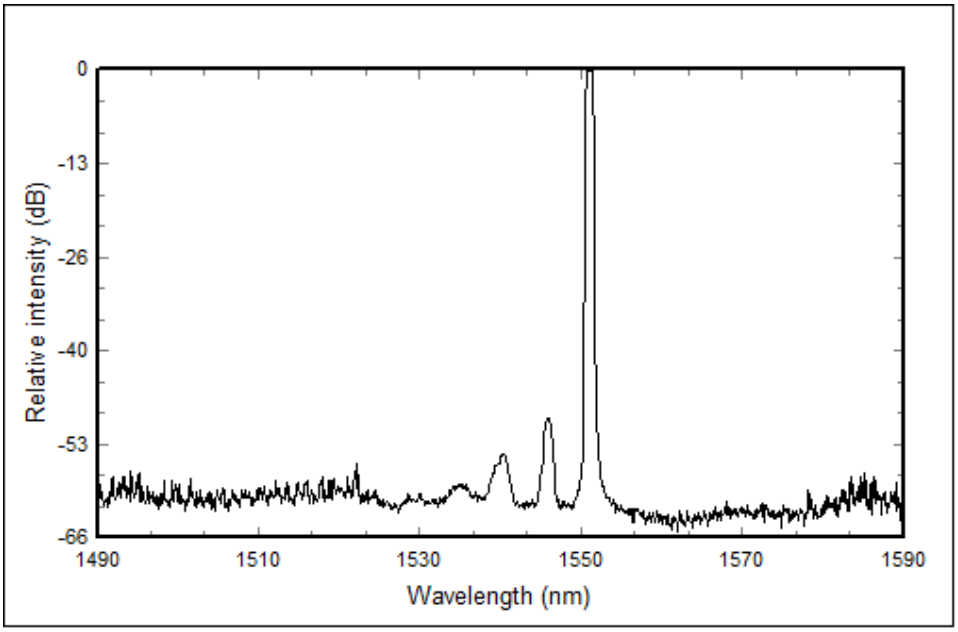

Figure 5.Spectrum of SC InP VCSEL.

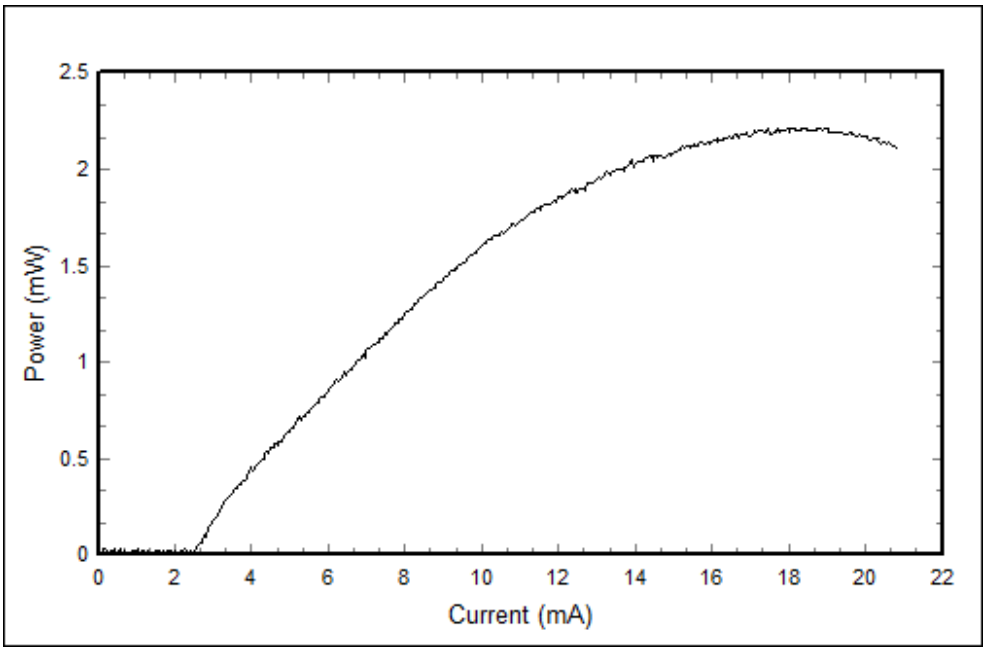

Figure 6. LIV curve of SC InP VCSEL.

1.5 VCSEL Assembly and Test

Subsequent VCSEL assembly and integration tests with SiP chips are in preparation and will be performed by and with project partners in the second half of 2019.

1.6 VCSEL Samples for Project Partners

During period 1 of the project, several batches of VCSEL samples have been supplied to project partners. This enabled the verification of integration and system performance testing.

1.7 VCSEL Stability and Reliability Analysis

A reliability test concept has been developed, stress test aging boards assembled and prepared for testing of future devices.

1.8 VCSEL and VCSEL Driver Evaluation

Within PASSION, a VCSEL driver has been identified to enable a high performance DMT operation of the VCSELs. To support the testing of the VCSEL driver together with the VCSELs, an evaluation board has been acquired. VCSEL bare dies have been mounted as close as possible to the driver chip following a proper developed procedure.

1.9 VCSEL package for Lab Evaluation

In order to perform VCSEL testing also in a lab setup, a high data rate TOSA package (Fig. 7, on the left and in the center) is being developed.

To connect the pins of the TO can to RF connectors, an adapter board (Fig. 7 on the rigth) will be manufactured.

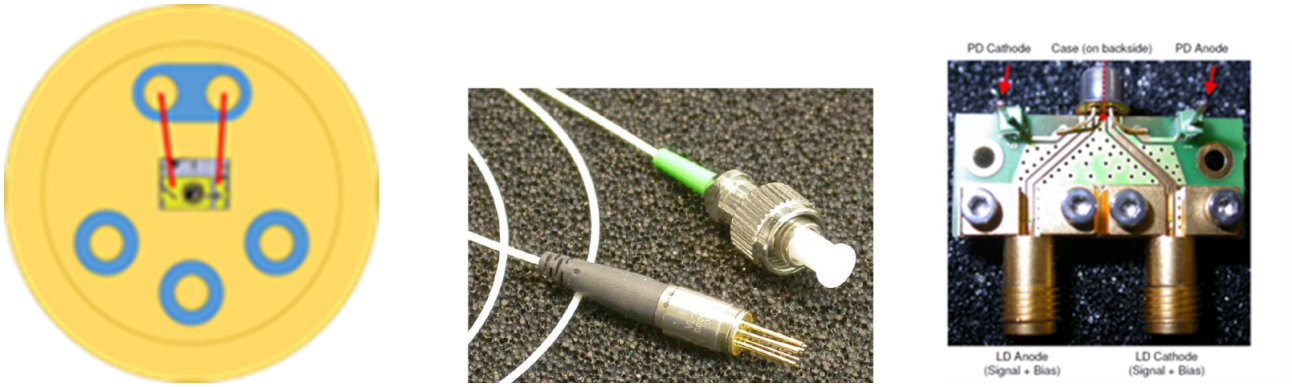

Figure 7. TO drawing (on the left). Pigtail TOSA (in the center), RF adapter board (on the right).

CONCLUSIONS

In this deliverable, the processes and methods developed by VERT to target the PASSION requirements for VCSELs are detailed.
In order to cover a wavelength span of 32 nm VERT has developed techniques to control the target wavelength of multiple wafers and a variation across one wafer both on 3" and 2" epitaxy equipment, applying complex measurement equipment and procedures. In a first wafer run, Vertilas manufactured a 3" wafer and was able to meet the target wavelength with an accuracy of around 2-3 nm.

The VERT VCSEL design has been adapted to minimize electrical power consumption, optimize the modulation 3 dB bandwidth to around 20 GHz and provide sufficient optical power, maintaining excellent single mode behaviour, high SMSR and wafer yields. The design optimizations included the MQW active region modification and the resonator length and semiconductor mesa design review to balance the above-mentioned requirements. The basic VCSEL design requires a complex set of production steps, in particular due to the deployment of BCB etching process to reduce intrinsic parasitic of the semiconductor material. The first wafer run produced single mode lasers meeting the right wavelength around 1550 nm with an SMSR higher than 35 dB.

The limitations presented by the first run samples are being fixed refining the newly developed wafer-production processing steps. Characterisation of new wafers is in progress and further data will be available in the upcoming months.

ACRONYMS

BCB Bisbenzocyclotene
BTJ buried tunnel junction
DMT discrete multitone
FIB focused ion beam
InP Indium Phosphide
MBE molecular-beam epitaxy
MQW multiple quantum well
SC short cavity
SMSR side mode suppression ratio
SOI Silicon-Over-Insulator
VCSEL vertical cavity surface emitting laser
WDM wavelength division multiplexing