Test results from passive SiPh PICs integrated with VCSELs

Project title	**Photonics technologies for ProgrAmmable transmission and switching modular systems based on Scalable Spectrum/space aggregation for future agile high capacity metrO Networks**
Project acronym	**PASSION**
Grant number	**780326**
Funding scheme	**Research and Innovation Action - RIA**
Project call	**H2020-ICT-30-2017 Photonics KET 2017 Scope i. Application driven core photonic technology developments**
Work Package	**WP3**
Lead Partner	**TUe**
Contributing Partner(s)	**VERT, VTT, POLIMI, SMO**
Nature	**R**
Dissemination level	**PU (Public)**
Contractual delivery date	**28/02/2019**
Actual delivery date	**14/06/2019**
Version	**1.0**

History of changes

Version	Date	Comments	Main Authors
0.1	30/05/19	First draft	Oded Raz (TUe)
0.2	07/06/19	Second draft	Giovanni Delrosso (VTT)
0.3	10/06/19	Third draft	Chenhui Li (TUe)
0.4	12/06/19	Fourth draft	Oded Raz (TUe)
0.5	13/06/19	Quality review	Porcel (VLC)
1.0	14/06/19	Final	Raz (TUE) - POLIMI

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This project has received funding from the European Union's Horizon 2020 Research and Innovation Programme under Grant Agreement No 780326.

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EXECUTIVE SUMMARY

This report provides a detailed description of the design, fabrication and testing of the co-integration of VCSELs with passive SiPh PCIs developed in the PASSION project.

The PASSION architecture, and in particular the silicon photonics chip design, the VCSEL characteristics and the preferred assembly strategy are taken into account. Next to the main assembly approach which assumes top reflecting mirrors and hence VCSEL assembly on the top of the SiPh PIC, also the embedding of the VCSELs in the substrate underneath the SiPh circuit has been investigated. The results of both assembly strategies indicate feasibility for assembly and initial insertion loss measurements for the top assembly strategy of below 5dB are very promising.

While the consortium has clearly opted to pursue the top assembly strategy, investigation of bottom assembly will continue as a risk mitigation effort and out of scientific curiosity.

1 INTRODUCTION

This report will provide a detailed description of the design, fabrication and testing activities which were taken in order to test the performance of light coupling between the Vertilas VCSELs and the VTT SiPh platform. The details concerning the design considerations for the VCSEL and the SiPh PIC have been included in *D3.1 Detailed design of the Tx module architecture and interfaces*.

The co-packaging of VCSELs and SiPh waveguides needs to address several different technological challenges. These include but are not restricted to:

- The optimal coupling of light from the large aperture of the VCSEL into the relatively narrow waveguides and the associated losses incurred or remedies which can be offered to overcome this losses.
- The proper electrical wiring (metal traces) needed to carry high speed signals from the VCSEL drives (See D3.1 & D3.2) to the VCSEL with maximal fidelity on top/bottom of the SiPh chip.
- The thermal conditions in which the VCSEL are operating depending on their position relative to the SiPh waveguides.

After a recap of the Tx architecture adopted in PASSION in Section 2, we report in Section 3 the results of the assembly of both top and bottom coupled VCSELs to the SiPh emphasizing the processing related aspects which led to the assembled test devices. In Section 4 the first experimental tests of the optical coupling between the VERTILAS VCSELs and the VTT SiPh waveguides are presented. The results presented in this Deliverable D3.4 constitute the achievement of the Milestone MS7 “Efficient coupling demonstrated between VCSELs, SiPh PICs and fibers”.

2 PASSION TX ARCHITECTURE

In this section we describe the PASSION Tx architecture in terms of design, VCSEL operation and target performances to justify the requirements required to the VCSEL drivers in order to be employed in the Tx implementation.

2.1 VCSEL SOURCES

In PASSION project, the VCSEL devices are developed and produced by the partner VERTILAS with the following targets:

- Single-mode operation;
- low power consumption < 35mW
- output power about 4 mW @ 20°C
- bandwidth S_{21} = 20GHz
- layout optimized for flip chip bonding
- far field FWHM < 12°

- SMSR > 35dB
- low threshold current I_{th} < 2.5 mA @ 20°C

The high modulation bandwidth (up to 20 GHz) requires to adopt a short-cavity design, achieved by means of a very short resonator length and an active region optimized for high bandwidth, as shown in Figure. 1. Such a bandwidth allows to directly modulate the VCSEL in order to achieve up to 50-Gb/s signal rate per each VCSEL, by exploiting DMT or PAM modulation (e.g. 4-PAM modulation).

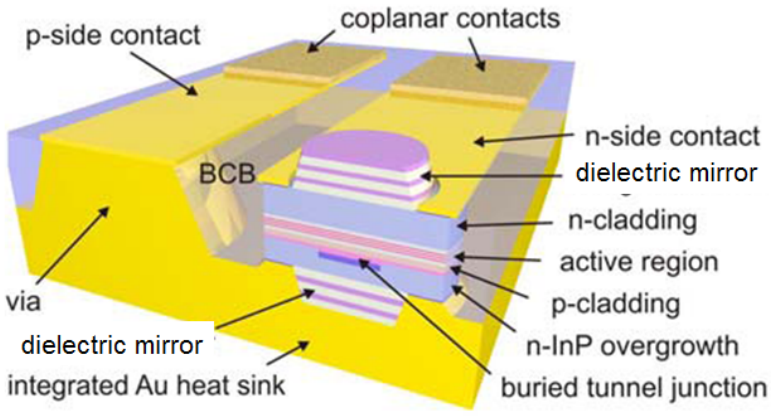


Figure 1. Cross section of the short-cavity VCSEL optimized for high modulation bandwidth.

For the realization of the PASSION Tx, VCSEL emission is required to cover the whole frequency range from 191.9 THz (corresponding to the ITU-T WDM channel CH19 at 1562.23 nm) to 195.9 THz (CH59 at 1530.33 nm). Long-wavelength emission is usually critical owing to laser heating due to poor thermal conductivity and increased thickness of long-wavelength DBRs as well as the stronger temperature dependence of the threshold current. VERTILAS approach overcomes these problems by employing a high-reflective and thermally well-conducting hybrid metallic/dielectric mirror together with a buried tunnel junction (BTJ) to enable low-resistance lateral current confinement and waveguiding. BTJ active area is maintained small (<5.5 μm) to optimize the SOI waveguide coupling in the PASSION Tx design. Figure. 2 shows the BTJ-based VERTILAS VCSEL structure with an emitted circular Gaussian laser beam spot with about 5.5 μm diameter (expected far field 10° to 12° FWHM).

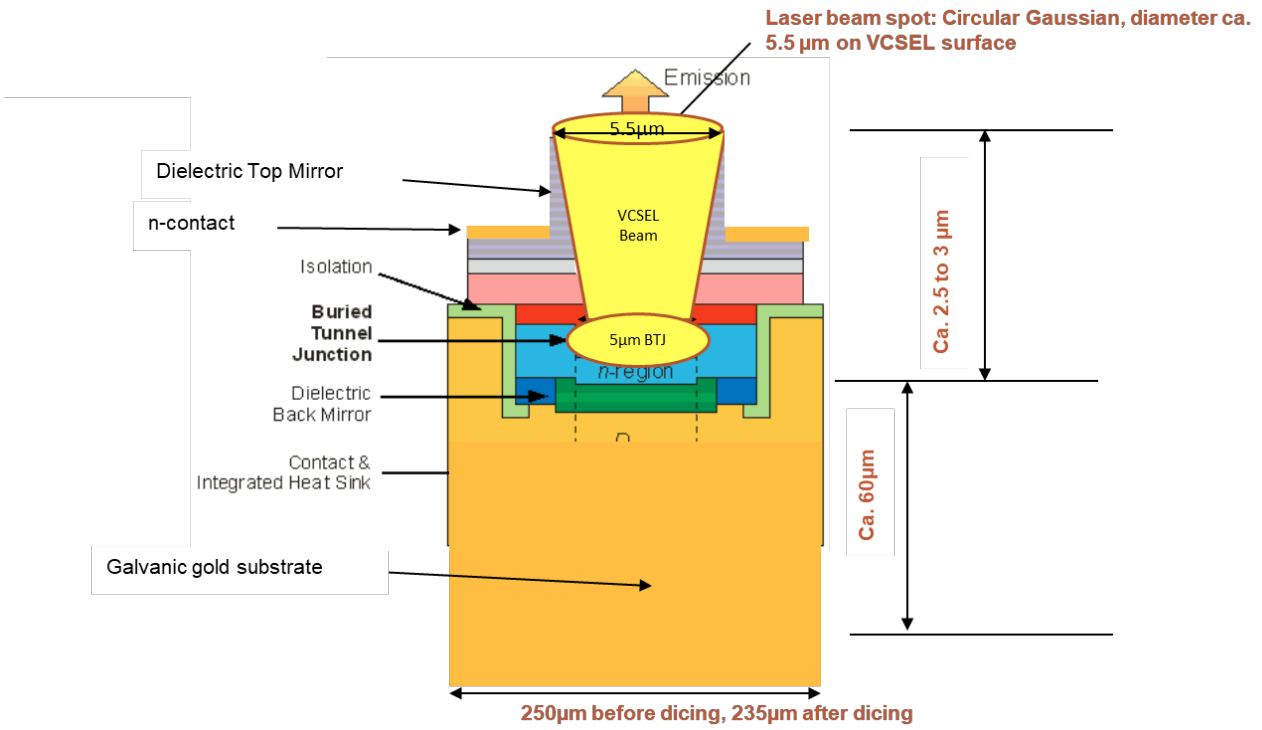


Figure 2. BTL-based VCSEL structure.

The PASSION approach requires that each VCSEL could be finely tuned in a 25-GHz channel grid to match with the design of the WDM multiplexers. To satisfy this requirement the VCSEL will be designed to target different emission wavelengths covering the C-band with 100-GHz spacing and further tuning over the 25-GHz grid will be achieved through current tuning.

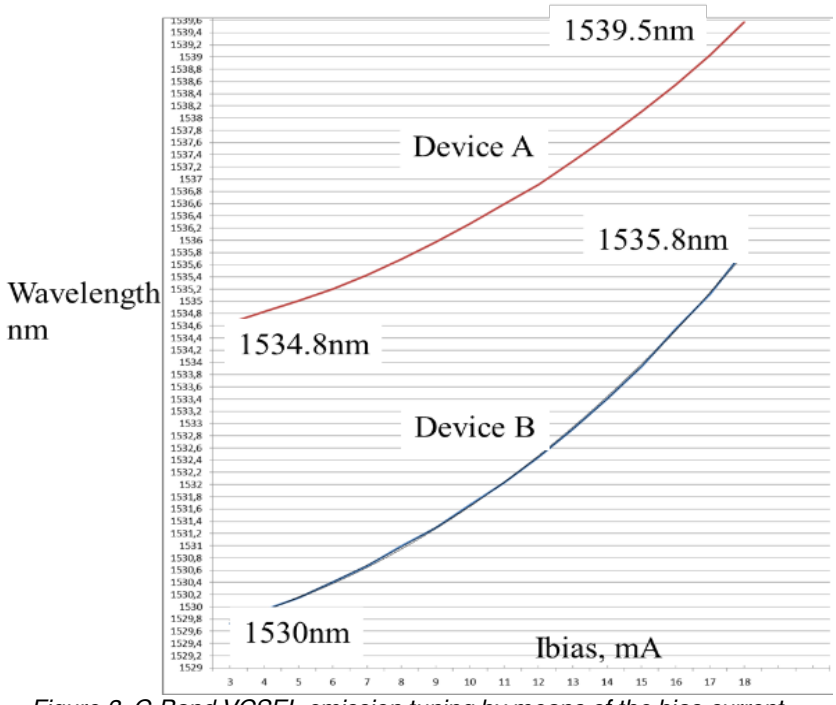


Figure 3. C-Band VCSEL emission tuning by means of the bias current.

A wide wavelength tunability is in fact performed in the VCSEL by changing the bias current, as demonstrated in Figure. 3 for two different devices A and B (during PASSION project new devices will be developed, improving present design to obtain the target bandwidth). The current tuning coefficient of the VERTILAS VCSELs is 0.1/0.2 nm/mA, dependently by the design and by the applied current. Also temperature wavelength stabilization is foreseen (temperature tuning coefficient is ca. 0.1 nm /°K). Moreover, Figure. 4 shows the operation of the VERTILAS VCSEL as a function of the bias current. To exploit the full S21 bandwidth, the I_{bias} should satisfy the relation $\sqrt{I_{bias} - I_{th}}$= 2.5/3 achieving the maximum modulation bandwidth.

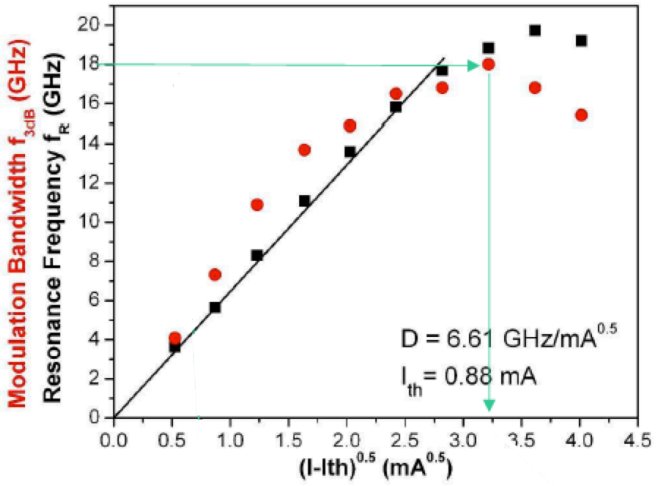


Figure 4. Modulation bandwidth (red circle) and resonance frequency (black square) as a function of the Ibias. Maximum bandwidth is achieved at I_{bias} of about 11-11.5 mA, corresponding to $(I-I_{th})^{0.5}$=3.24 (I_{th}=1 mA).

2.2 PASSION MODULAR APPROACH

One of the main objectives of PASSION project is the development and deployment of a photonic Tx to support agile metro networks, capable of enabling target capacities higher than Tb/s per spatial channel, higher than 100 Tb/s per link and Pb/s per node by means of spectral and spatial aggregation. PASSION's goal is achieved by exploiting VERTILAS VCSEL sources, described in the paragraph 2.1, each one operating at a different 25-GHz spaced WDM wavelength in the C-band, directly modulated to obtain up to 50 Gb/s rate, to target up to 8-Tb/s WDM aggregated capacity at a single polarization. 16 Tb/s per spatial channel are achieved exploiting polarization-division multiplexing, while the spatial dimension of 7 cores MCF or 7 fibers in a bundle allows enabling up to 112 Tb/s aggregated capacity per link.

This objective is pursued with a modular approach as shown in Figure 5. A 40-VCSEL based module is built by integrating 4 sub-modules, each one containing 10 VCSELs. The 40 emission wavelengths cover the entire C-band with 100 GHz granularity and are fine-tuned in a range of 0-75-GHz through the VCSEL bias current and stabilized by a temperature cooler. By 50-Gb/s modulation of each VCSEL, an aggregated capacity of 2 Tb/s per module is achieved. By combining four of such a module with external inter-leavers a full 160-ch Tx super-module (characterized by 8 Tb/s capacity) is obtained with 25-GHz wavelength granularity. This type of modularity offers the ability to fabricate and stock only one module type, and to use the identical 40-ch modules to build the full 160-ch Tx super-module. Then, a discrete polarization multiplexer combines inputs from two identical 160-ch

Tx super-modules to get 16 Tb/s capacity. Finally, signals are coupled to multi-core fibers or fiber ribbons using spatial multiplexers for the fully equipped S-BVT (112-Tb/s in capacity).

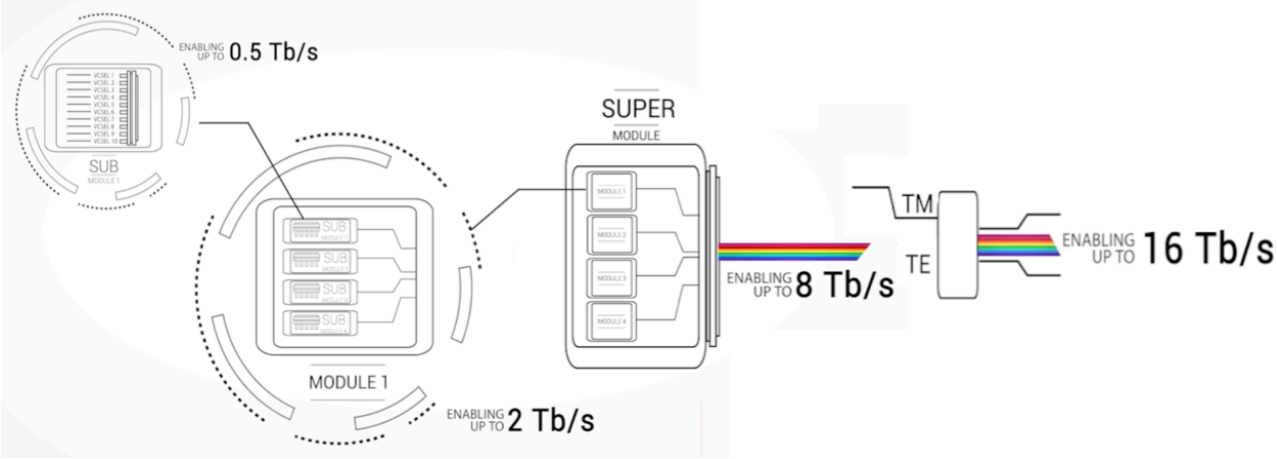


Figure 5. Example of Tx module capacity aggregation exploiting the spectral and space dimensions.

2.3 SILICON PHOTONICS CHIP DESIGN

The module structure representing the smallest discrete granularity element in PASSION aggregation modular approach is shown in Figure. 6. The structure includes:

- 1 x SOI PIC embedding 40 channels (100-GHz spaced), 4 x10 input channels (400GHz spaced) optical multiplexers (MUX#1-4) having their respective outputs furthermore multiplexed into MUX#5 whose output represents the exit port to couple light into a pigtailed single mode polarization-maintaining fibre (PMF) assembly.
- 40 x VCSEL chips (directly modulated up to 50Gb/s each)
- 40 x linear VCSEL driver chips
- 1 x Land Grid Array (LGA) redistribution layers (RDL) fan-out electrical interposer, embedding 2 differentiated thermal sinking paths able to separate heat flows generated by VCSELs (which require an active cooling set a 40°C ± 0.1°C) from the thermal payload generated by linear drivers (which can be passively dissipated in air with a standard heat sink design).

As reported in the Deliverable D3.1, VCSEL drivers are put outside the Si-PIC chip for thermal reasons, but still at very short distance allowing wire bonds (WBs) to provide interconnections, as shown in Figure. 7 left. However, for high-speed and high bandwidth operations WBs have to be as short as possible (preferably <200μm). VCSELs are positioned as close to the Si-PIC chip edge as possible. The chosen solution is to place the 40 VCSELs, (which correspond to the 40-channels requirement of the Si-PIC chip), close to the perimeter of the SiPh chip with 10 VCSELs on each edge, as shown in Figure. 7 right.

With this architecture, the channel pitch, which is the physical spacing between the adjacent channels on any given edge of the chip, influences the chip size. In fact, the channel pitch is dependent on the pitch among the following elements: the multiplexer input arms, the VCSELs, and the drivers. Consequently, the maxima of these elements decide the final pitch. We need thus VCSEL driver dimension to not exceed the range of 1.5-2 mm. In this way the channel pitch value of 2 mm will be obtained, taking into consideration that some additional space is needed for the output fibre placement, the chip size should be expected to be around 20 x 20 mm^2.

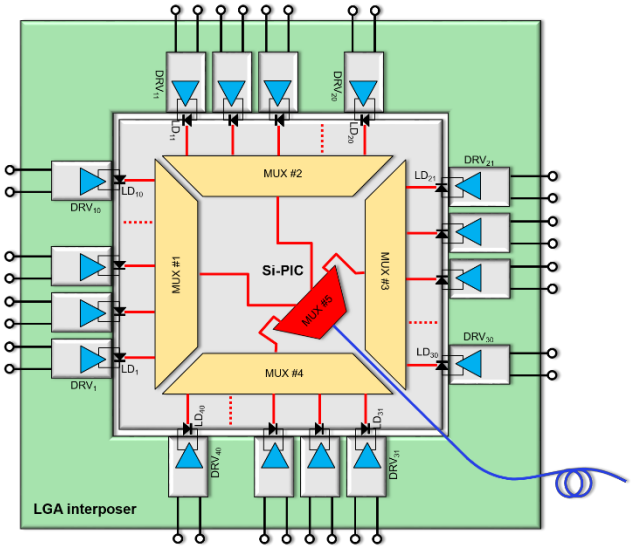


Figure 6. 40-VCSEL module structure.

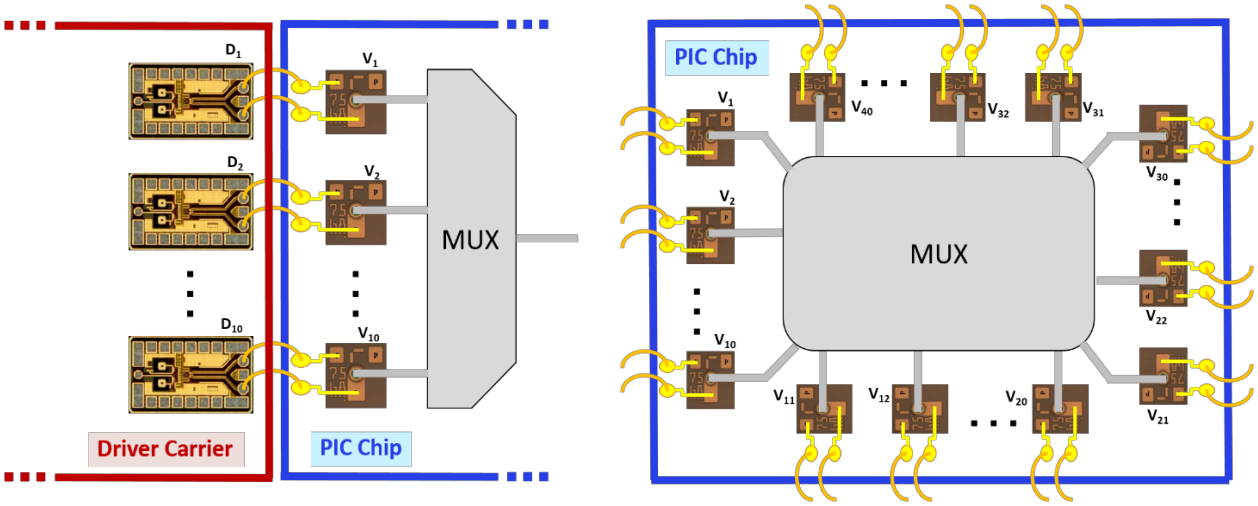


Figure 7. Module integration scheme: integration of VCSELs and drivers (left). Designed VCSEL arrangement on a 20x20 mm² PIC chip (right).

3 CO-INTEGRATION OF VCSELS AND SIPH PIC

In this section we describe the steps taken in order to accomplish the co-integration of the Vertilas VCSELs and the VTT SiPh PIC. Next to the details of the assembly and fabrication steps related to the top illumination approach (selected as primary strategy in the project), we will also give details of results of the alternative approach which aims to use bottom illumination.

3.1 FABRICATION AND ASSEMBLY STEPS LEADING TO CO-INTEGRATION OF VCSELS ON TOP OF SIPH MIRRORS

The traditional way to couple light from end-firing waveguides of Si-Photonic Integrated Circuits (Si-PICs) whether performed with fibers or free-space optics, although broadly in use has shown its limits in scalability, reliability and assembly costs. Those limitations greatly motivated in PASSION the exploitation of total internal reflection-based mirrors (TIR) concepts in combination with VTT 3µm SOI waveguides platform to perform optical coupling with other chips (i.e. VCSELs and detectors) directly on top of the wafer surface exploiting Wafer-Level Packaging (WLP).

TIR mirrors provides the highest possible reflection coefficient at any wavelengths, a broadband functionality and are independent of fabrication tolerances. Furthermore, this is ideal for accessing device´s performance with an E/O Wafer-Level Testing (WLT) setup.

Standard Si etch plane produces a 54.7°angled surface which doesn't allow to get a TIR condition and the mirror surface is dependent on the fabrication misalignment leading to coupling loss variations from device to device, wafer to wafer, and run to run. However, under special etching conditions, a 45° vertical coupling TIR mirrors have been realized at VTT in combination with a 3 µm SOI waveguides [5]. A SEM, FIB and schematic cross-section images are shown in Fig 8.

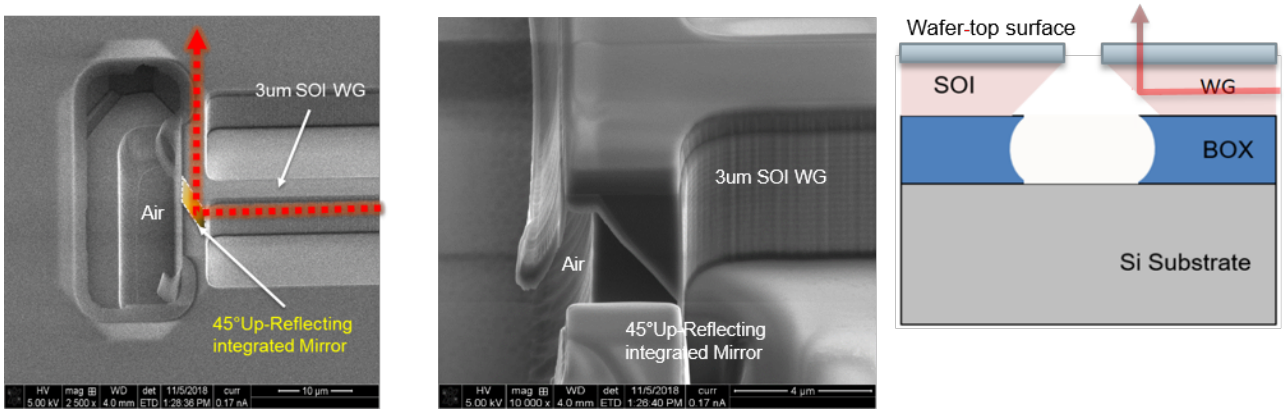


Figure 8. A SEM and FIB cross-section of a 45up-reflective TIR mirror coupled with a 3µm SOI WG.

In the 2Tb/s MOD1 Si-PIC the process to realize Up-Reflective mirrors has been used to realize the coupling system between each (of the forty) VCSEL lasers and its related waveguide (WG). Similarly, the Up-Reflective mirrors have been used also for the output optical port and as well as for PD monitors (Fig.9).

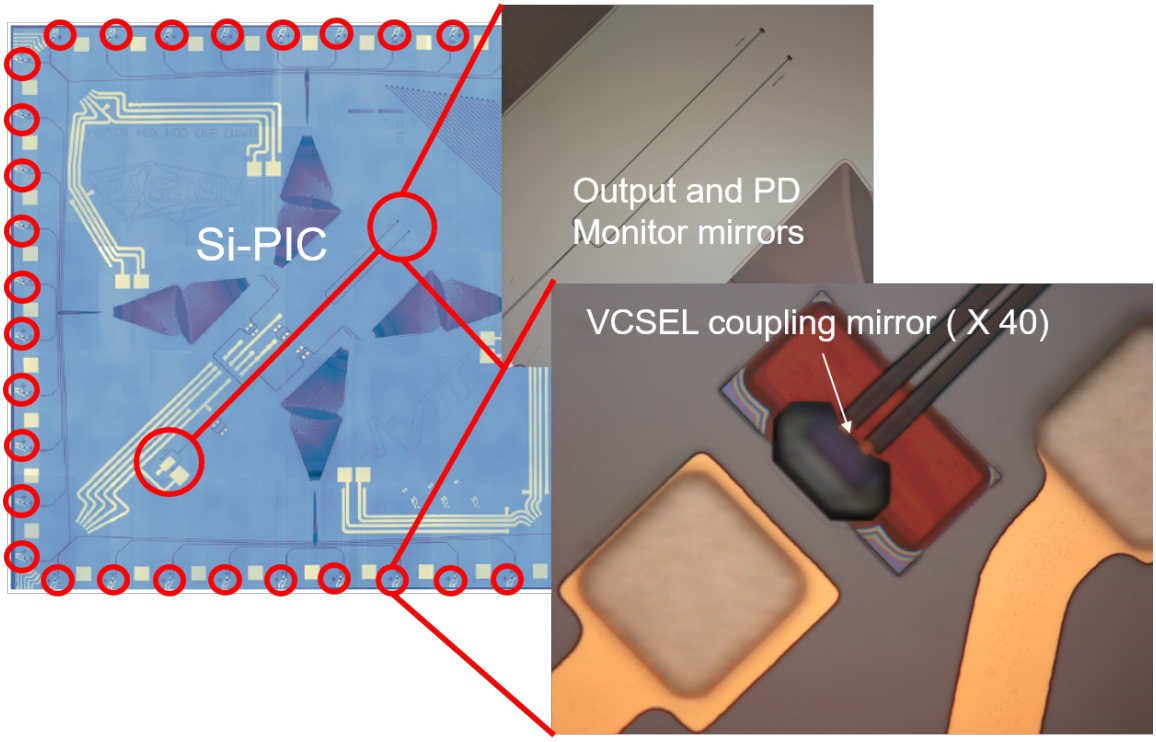


Figure 9. Up-Reflective Mirrors location on MOD1 Si-PIC

Based on detailed information on VCSEL geometry provided by VERTILAS and further profilometric analysis performed at TuE a precise topographic map of the VCSEL chip to be used in PASSION has been carried out. Particularly relevant was the precise estimation of the height-gap between the VCSEL P-N pads and the top surface of the dielectric mirror as shown in Fig.10. This gap has been measured to be around 3 μm and has been taken in account to design the solder pad geometry and solder metallurgies on the mirror top surface.

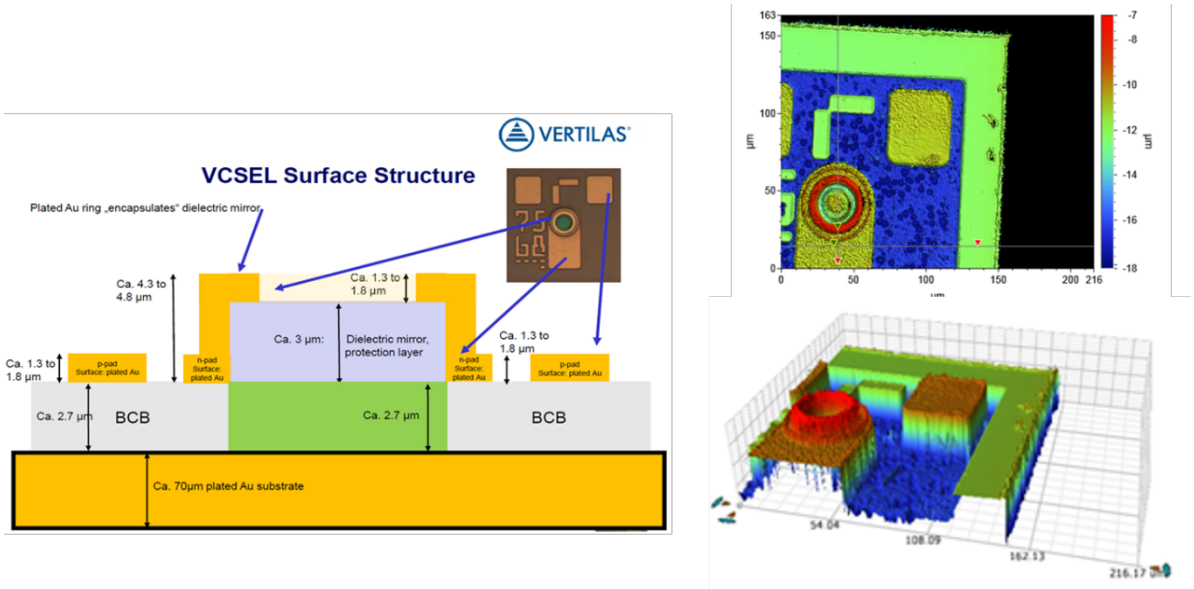


Figure 10. Topographic and profilometric analysis of VCSEL chip to be flip-chip bonded on up-reflective mirrors

During flip-chip bonding operations, the desired gap between the dielectric mirror and the mirror top surface has been kept to a safe minimum value with the aim to mitigate additional coupling losses due to VCSEL extra beam divergence and the risk to have a dielectric mirror´s catastrophic damage if in physical contact after bonding, with the mirror top surface. Therefore, the solder pads in the Si-PIC have been designed to be slightly higher than 6μm before bonding (Cu ≥2μm+Ni ≥2μm+Sn 2μm). After bonding the 2μm Sn will melt together with the VCSEL.

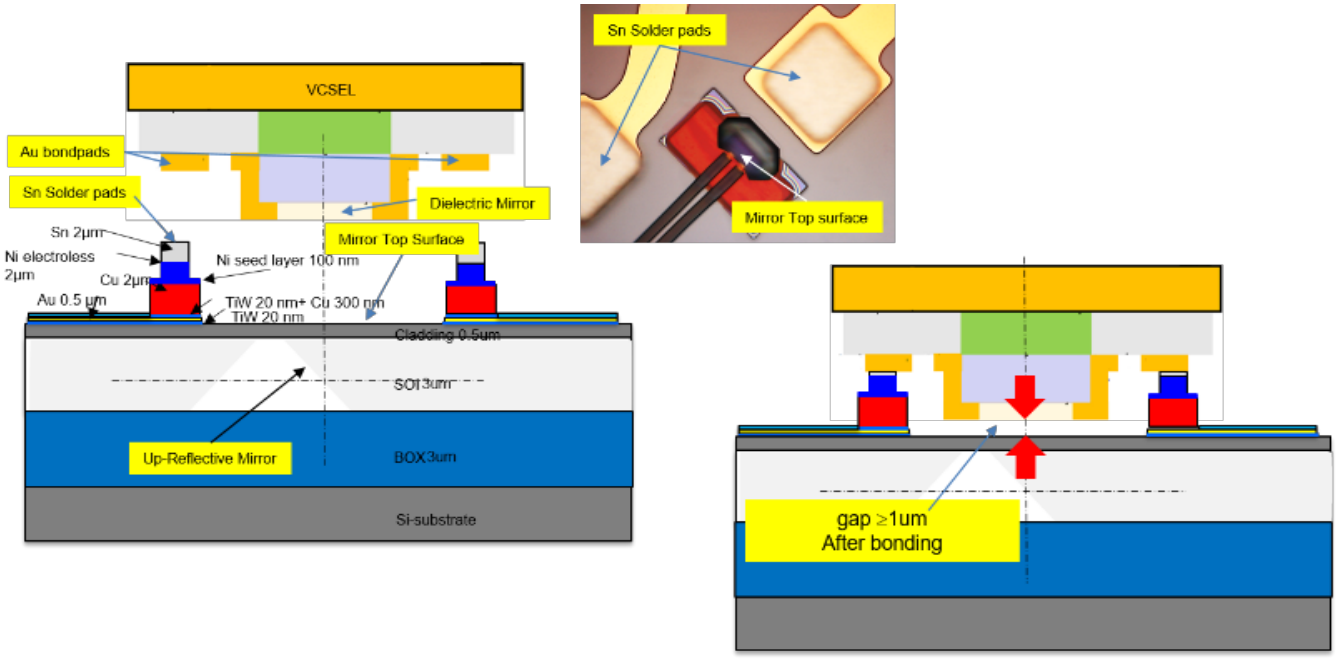


Figure 11. Cu-Ni hard stoppers allowing >1μm air gap between VCSEL dielectric mirror and up reflective mirror top surface

Au bond pads leaving the ≥4μm Ni+Cu thickness to behave as a hard stopper to safely assure ≥1μm air gap between the Dielectric mirror and the mirror top surface (Fig.11).

Finally, a simple and initial bonding test has been performed by passive-aligning and flip chip bond a VCSEL chip in position on top of Up-Reflective mirror as shown in Fig. 12. Solder bonds have been performed at 230C in free air with a manual bonder and a temperature controlled chuck.

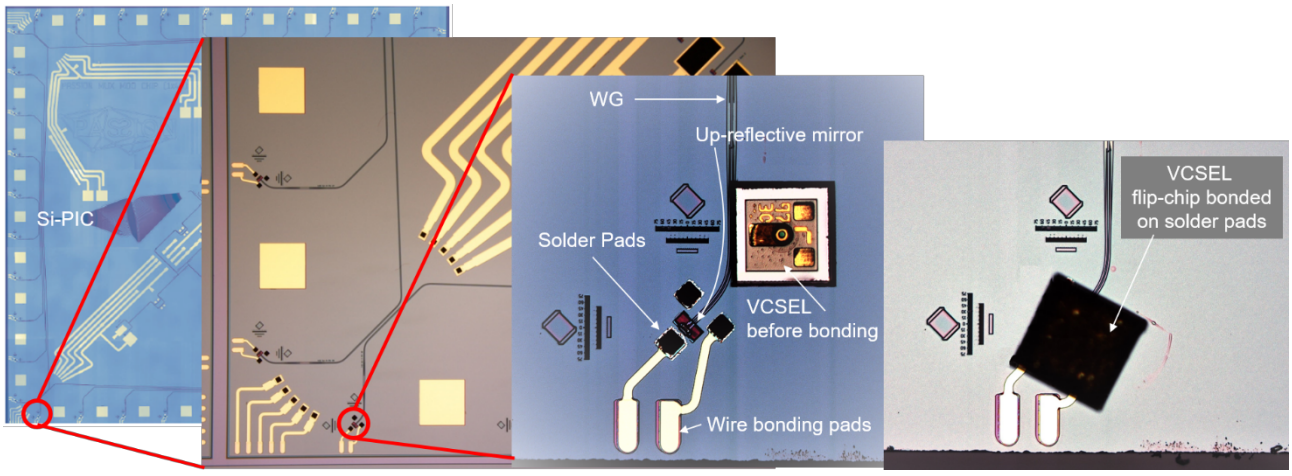


Figure 12. VCSEL Flip Chip bond on Up Reflective mirror and solder pads

3.2 FABRICATION AND ASSEMBLY STEPS LEADING TO CO-INTEGRATION OF VCSELS BELOW THE SIPH MIRRORS

As an alternative, VCSELs are also considered to be co-integrated with down reflecting mirrors, which is developed by VTT as well. The package scheme is proposed and shown in Figure 13. The VCSEL is embedded in the silicon substrate through backside process and flip-chip bonding. Electronic circuits are accordingly designed and fabricated on the backside, and the emitted light is coupled with the down reflecting mirror through the BOX layer.

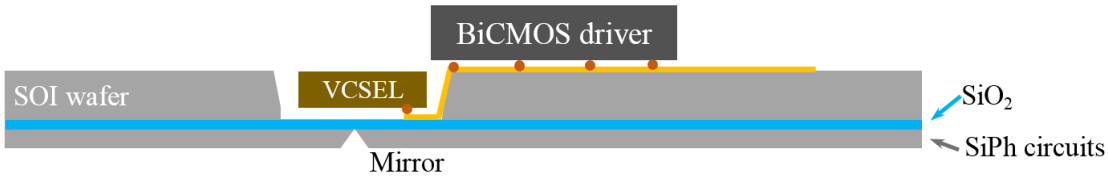


Figure 13. Integration scheme of VCSELs and down reflecting mirrors.

There are several advantages of this integration scheme. Firstly, the down reflecting mirror is easier to fabricate. Secondly, the electronic circuits and photonic circuits are separately designed on both sides of the wafer. Thirdly, the shorter distance between BiCMOS driver and VCSEL can be realized to ensure the sufficient RF performance.

In order to process on the backside of the SOI wafer, the wafer is thinned down to 300 μm and diced into 40 mm x 40 mm squire samples, which is illustrated in D3.3. Each sample includes four designs, and the channels located in the center will be processed.

The fabrication starts with PECVD SiNx as the hard mask for wet etching. Bottom side alignment and lithography are employed to transfer the alignment marker and make the square openings for silicon etching. After a long etching of silicon, a cavity is formed, followed by the seed layer sputtering and circuits plating. The process flow is demonstrated in Figure 14. Two photos in Figure 15 show the process steps respectively.

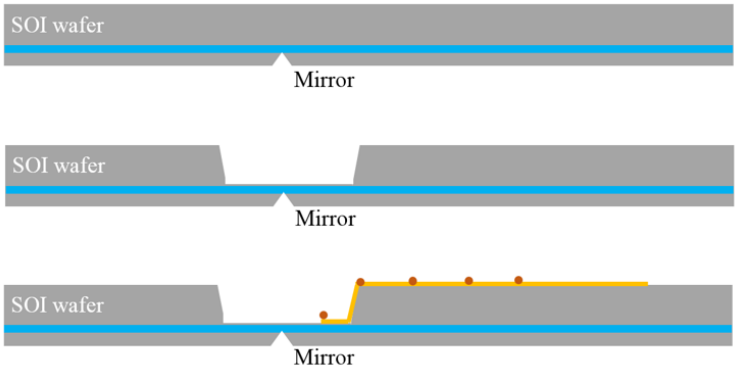


Figure 14. Back side process flow for integrating VCSEL on the back side.

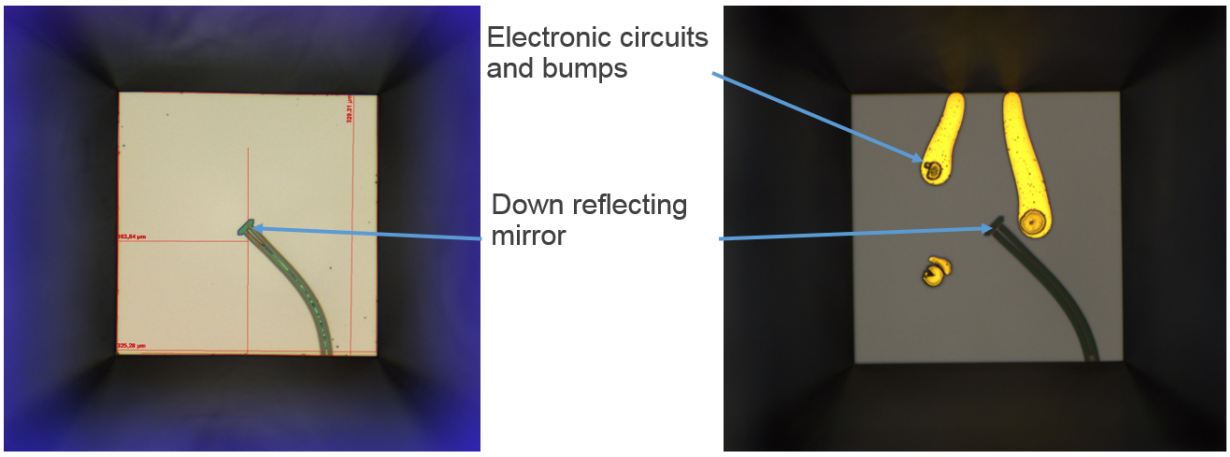


Figure 15. Microscope photos focus on the bottom of the cavity. Left: after silicon etching process, the waveguide can be seen through the BOX layer. Right: after plating process, circuits plating and pads plating.

Flip-chip bonding is tested after the fabrication process, as shown in Figure 16. VCSEL is firstly aligned with PIC sample by aligning the aperture with the end of waveguide (mirror). However, the membrane broke during the bonding process. This is due to the strength of the thin BOX layer.

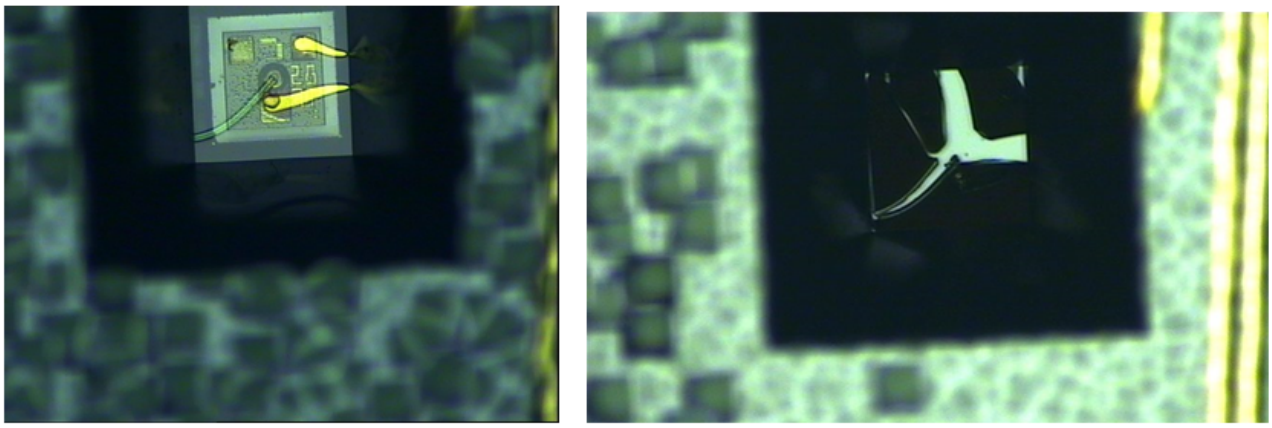


Figure 16. Microscope photos are taken during flip-chip bonding process. Left: VCSEL is aligned with the down reflecting mirror. Right: after process, the membrane broke.

An alternative process is also proposed and tested. Instead of etching until the BOX layer, a thin silicon layer is left un-etched to support flip-chip bonding of VCSEL and compensate the extra height of VCSEL. The updated scheme is shown in Figure 17, and the process results are shown in Figure 18. In this case, the un-etched silicon layer is too thick to etch an optical via through, and a better layer arrangement can be achieved by controlling etching rate of silicon process. The thickness of the silicon we will target is 10 μm. In the long run, a focus lens needs to be designed. In this way, the beam from VCSEL can be collimated, and the thin silicon layer can be used to support the flip-chip bonding process.

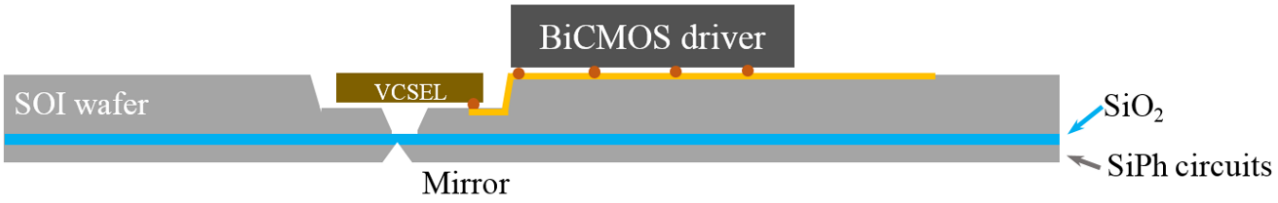


Figure 17. The updated assembly scheme, a thin layer of silicon is remained to support the flip-chip bonding. One step more to define the optical window.

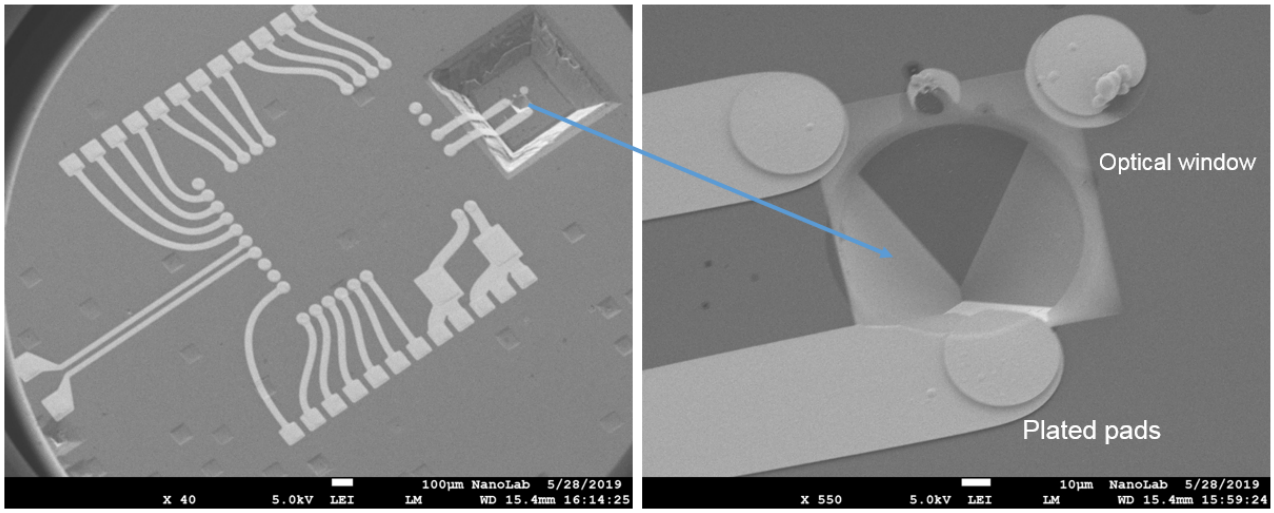


Figure 18. SEM photos after process. Left: the electronic circuits for VCSEL and its driver. Right: zoom in photo of etched optical window.

4 EXPERIMENTAL TESTING OF LIGHT COUPLING FROM VCSELS TO PASSIVE SIPH PICS

In this section, we will give the initial results of the experiments performed to test light coupling between VCSELs and passive SiPh PICs.

4.1 TOP SIDE ASSEMBLY

In Fig. 19 a measurement set-up has been built to obtain the optical reference power to be coupled into up-reflective mirrors. A 1.55 μm broadband source and an optical power meter are respectively connected with a single mode lensed fiber, designed to match the Mode Field Diameter of 3μm SOI WGs (MFD approx=2.8μm) integrated into the Si-PIC. After fiber to fiber alignment and power optimization, an I.L. of 3.8 dB was obtained. This reference value shall be deducted from the total I.L. values measured for mirror-to-mirror or VCSEL-to output mirror transitions, in order to calculate the final I.L. of each transition.

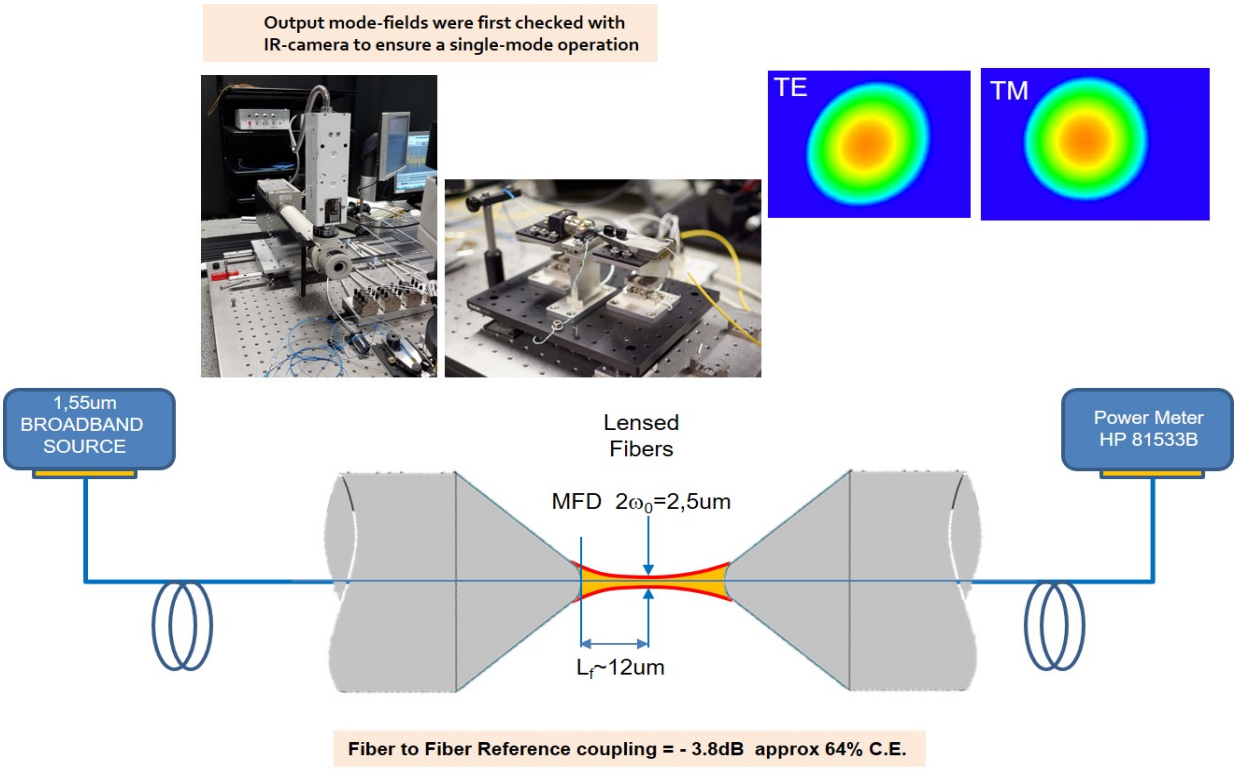
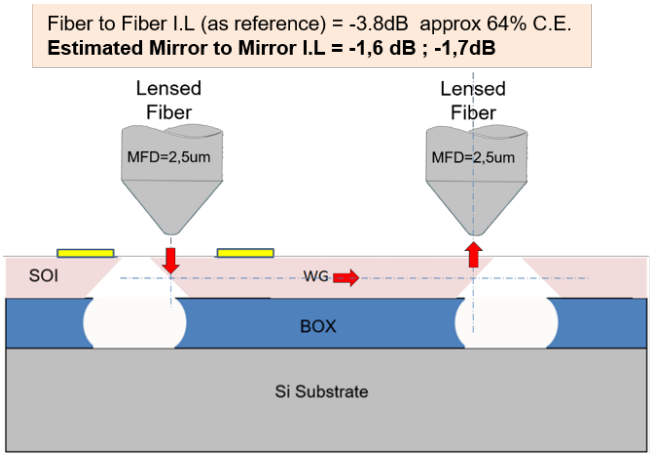


Figure 19. Setup to obtain the optical reference power to be coupled into up-reflective mirrors

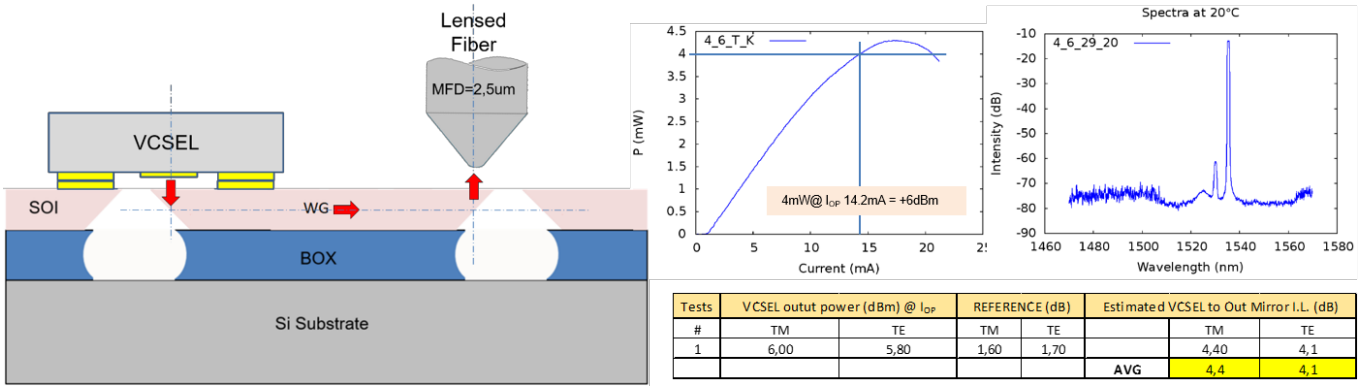
In the same setup a PASSION MOD1 Si-PIC has been therefore mounted and tested. The approach used and the number of coupling tests performed to get a reasonable statistics are shown in Fig 20. After 18 mirror-mirror´s coupling tests and deducting the reference power level (-3,8dB for TM and -3.95 for TE), an average value of 1.7dB (TE) and 1.6dB (TM) have been obtained.

Furtherly, a VCSEL laser has been flip-chip bonded and coupled to an SOI WG as shown in Fig.21. The VCSEL has been powered to an operating current I_{OP} =14.3mA corresponding to a +6dBm output optical power and coupled into a mirror-WG-output mirror transition as shown in Fig. 21 and Fig 22. A coupling loss of 4,1dB (TE) and 4, 4 dB (TM) have been obtained.



Tests	Mirror to Mirror coupling losses (dB)		REFERENCE (dB)		Estimated Mirror to Mirror I.L. (dB)		
#	TM	TE	TM	TE		TM	TE
1	-5,5	-5,8	-3,80	-3,95		-1,70	-1,9
2	-5,3	-5,6	-3,80	-3,95		-1,50	-1,7
3	-5,7	-6,0	-3,80	-3,95		-1,90	-2,1
4	-5,4	-5,7	-3,80	-3,95		-1,60	-1,8
5	-5,3	-5,6	-3,80	-3,95		-1,50	-1,7
6	-5,6	-5,9	-3,80	-3,95		-1,80	-2,0
7	-5,3	-5,6	-3,80	-3,95		-1,50	-1,7
8	-5,4	-5,6	-3,80	-3,95		-1,60	-1,7
9	-5,2	-5,5	-3,80	-3,95		-1,40	-1,6
10	-5,3	-5,6	-3,80	-3,95		-1,50	-1,7
11	-5,1	-5,4	-3,80	-3,95		-1,30	-1,5
12	-5,3	-5,6	-3,80	-3,95		-1,50	-1,7
13	-5,1	-5,4	-3,80	-3,95		-1,30	-1,5
14	-5,6	-5,8	-3,80	-3,95		-1,80	-1,9
15	-5,2	-5,5	-3,80	-3,95		-1,40	-1,6
16	-5,8	-6,1	-3,80	-3,95		-2,00	-2,2
17	-5,2	-5,5	-3,80	-3,95		-1,40	-1,6
18	-5,1	-5,3	-3,80	-3,95		-1,30	-1,4
					AVG	-1,6	-1,7

Figure 20. Set-up to measure Mirror-WG-Mirror I.L.



Tests	VCSEL outut power (dBm) @ I_{OP}		REFERENCE (dB)		Estimated VCSEL to Out Mirror I.L. (dB)		
#	TM	TE	TM	TE		TM	TE
1	6,00	5,80	1,60	1,70		4,40	4,1
					AVG	4,4	4,1

Figure 21. VCSEL-WG-Mirror I.L. measurement scheme

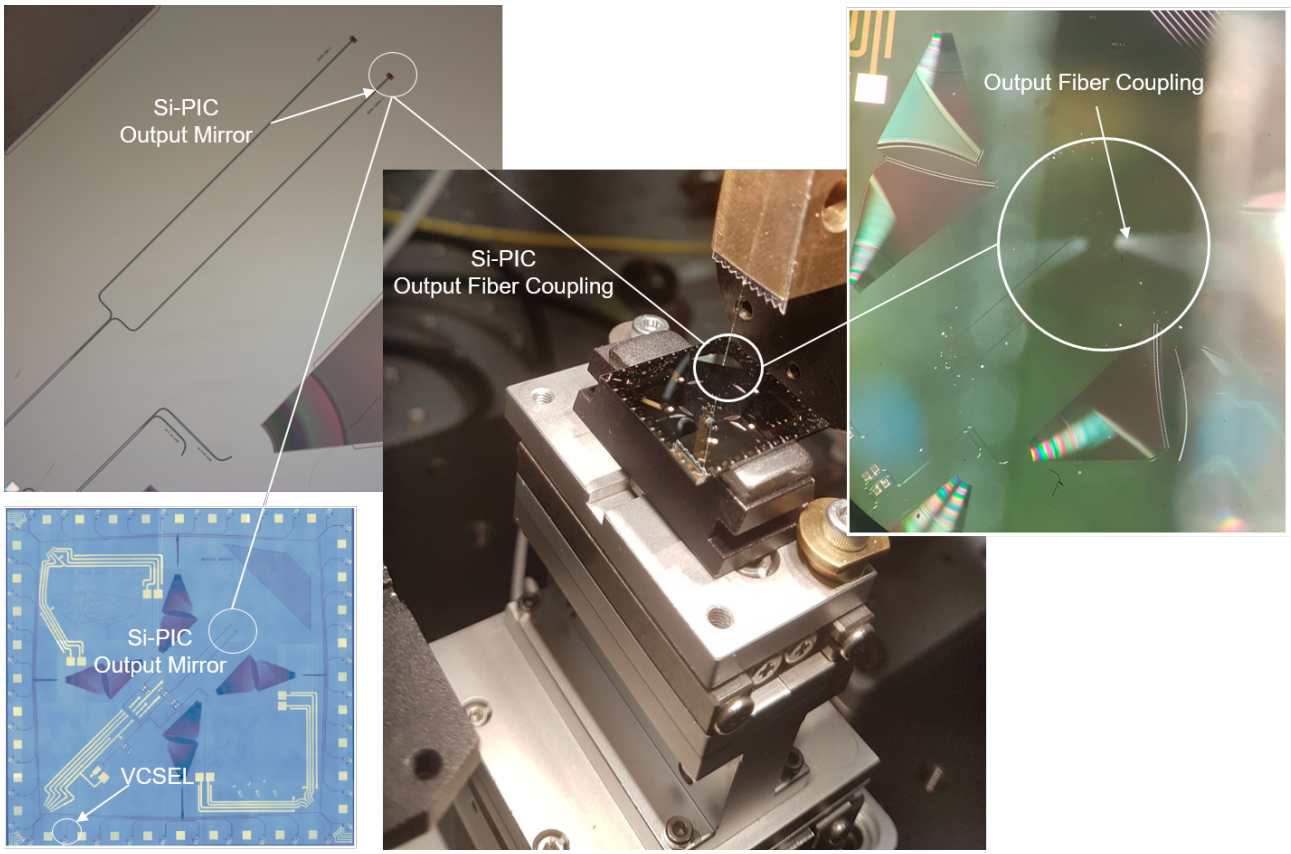


Figure 22. Set-up to measure VCSEL-WG-Mirror I.L.

4.2 BOTTOM SIDE ASSEMBLY – TESTING OF ELECTRIC CONNECTIONS

Flip-chip bonding and high speed modulation of VCSELs have been tested on a dummy silicon wafer. The same fabrication process, which will be used for a formal PIC sample, is followed and a thin layer of silicon is remained as proposed in Fig.17. Instead of using the down reflecting mirror, the prism light turn system (PLT) is used to couple the light in to optical fiber. In Figure 23(A) VCSEL and BiCMOS driver, which is specialized at 28 Gb/s are assembled, in Figure 23(B).

A 30 Gb/s non return to zero (NRZ) signal is fed by differential RF probes (signal-signal) through fan-out pads. The converted optical signal is detected by a by an oscilloscope fan out fibre. The eye

patterns is captured and shown in Figure. 23(C).

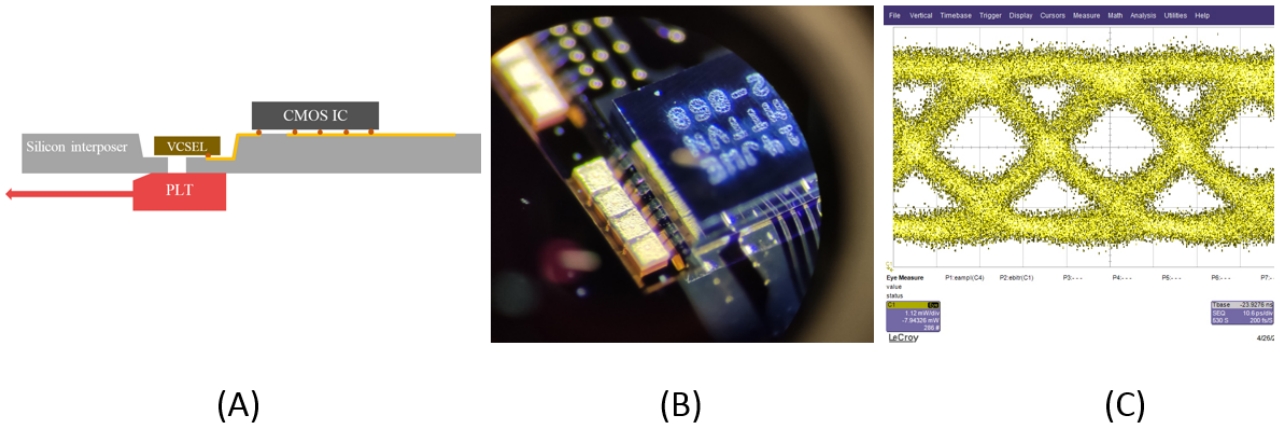


Figure 23. The testing process on a silicon wafer. (A) Similar scheme with PLT (B) flip-chip bonding of VCSEL and CMOS driver (C) optical eye pattern working at 30Gb/s.

5 CONCLUSIONS

In this deliverable, both schemes of assembling VCSEL on top side with up reflecting mirror and on bottom side with down reflecting mirror are explored. The fabrication process is completed, and VCSELs are flip-chip bonded. The light coupling test are also performed to evaluating the up-reflecting mirror. For the bottom assembly option, the performance of the short plated metallic traces between driver and VCSEL are included.

We have demonstrated that both assembly techniques are viable and have shown that insertion losses for a passively aligned VCSEL to a top facing mirror is below 5dB (4.4dB). We have also shown that by maintaining very short interconnections between driver and VCSEL, the Vertilas VCSELs can support 30Gb/sec NRZ modulation giving confidence that a 50 Gb/sec cumulative capacity is feasible using either PAM4 or DMT modulation techniques.

The results presented in this Deliverable D3.4 constitute the achievement of the Milestone MS7 “Efficient coupling demonstrated between VCSELs, SiPh PICs and fibers”.

6 REFERENCES

[1] A. Gatto, D. Argenio, P. Boffi, “Very high-capacity short-reach VCSEL systems exploiting multicarrier intensity modulation and direct detection,” Opt. Expr., 24, 12, 12769-12775 (2016).

[2] F. Li, et al., "Optimization of training sequence for DFT-spread DMT signal in optical access network with direct detection utilizing DML," Opt. Express 22, 22962-22967 (2014)

[3] P. S. Chow et al., "A practical discrete multitone transceiver loading algorithm for data transmission over spectrally shaped channels," IEEE Trans. on comm., Vol. **43**, pp. 773-775, (1995).

[4] A. Gatto, P. Parolari, C. Neumeyr, and P. Boffi, "Beyond 25 Gb/s Directly-Modulated Widely Tunable VCSEL for Next Generation Access Network," in OFC Conference, 2018, paper Th1E.2.

[5] S.Bhat, M.Harjanne, F.Sun, M.Cherchi, M.Kapulainen, A.Hokkanen, G.Delrosso, T.Aalto, "Low Loss Devices fabricated on the Open Access 3 µm SOI Waveguide Platform at VTT" in ECIO 2019, paper T.Po2.18.

ACRONYMS

4-PAM 4-level pulse amplitude modulation
BTJ buried tunnel junction
DBR distributed Bragg reflector
DMT discrete multitone
FWHM full width half maximum
LGA Land Grid Array
MCF multicore fibre
MUX multiplexer
OOK on-off keying
PECVD Plasma-enhanced chemical vapor deposition
PIC Photonics Integrated Chip
PLT prizm light turn system
PMF polarization-maintaining fibre
RDL redistribution layers
S-BVT sliceable bandwidth/ bit rate variable transceiver
SMSR side mode suppression ratio
SOI Silicon-Over-Insulator
TX transmitter
VCSEL vertical cavity surface emitting laser
WDM wavelength division multiplexing
WB wire bond