1 ANNEX I – D3.3 PUBLIC SUMMARY

In the PASSION project the development of the so-called MOD1 (the building block module combining 40 100-GHz spaced VCSELs to achieve a whole transmission capacity up to 2 Tb/s) relates to the integration of all optical functionalities into a Silicon-On-Insulator Photonics Integrated Chip (Si-PIC) (Fig. 1). All necessary building blocks combined on a single Si-PIC chip to form a full MOD1 architecture and the related mask designs, together with innovative integrated mirror designs have been successfully carried out.

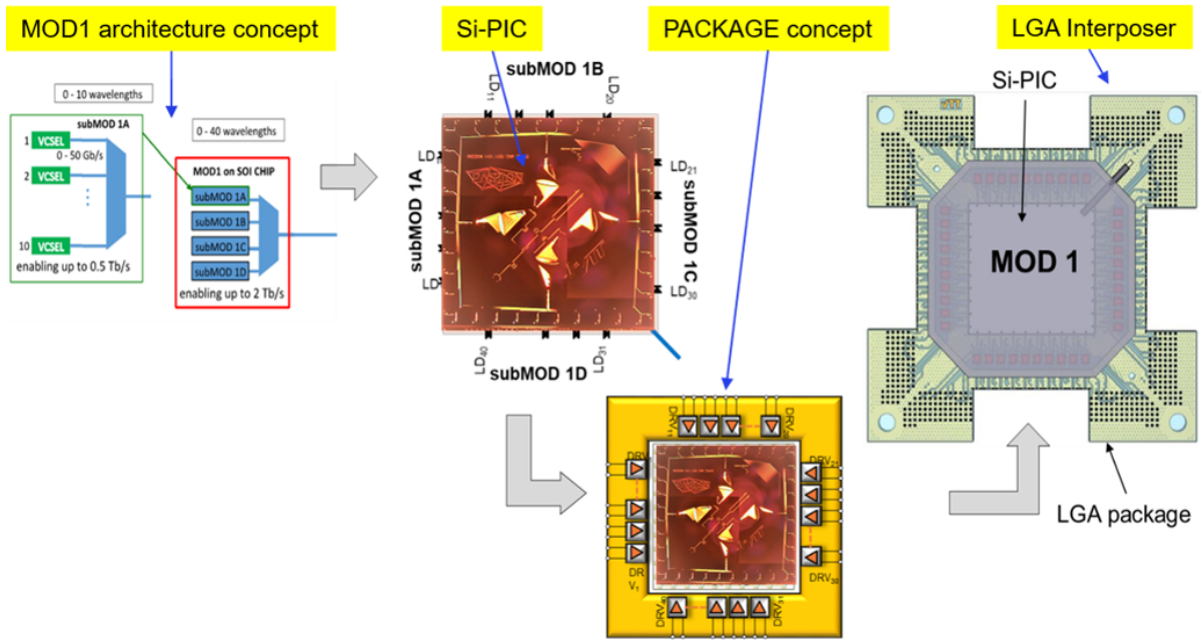

Figure 1 2-Tb/s MOD1 architecture and LGA interposer design.

To de-risk the optical design, alternative combinations of the multiplexer (MUX) elements necessary for achieving the MOD1 interleaving functionality have been undertaken. Initial characterizations of Arrayed Waveguides Gratings (AWGs) and Echelle Gratings (EGs) embedded in separate chips suitable for testing and benchmarking results have been performed. Testing results on EGs with insertion loss lower than 0.5 dB and cross-talk of -20 dB on the entire C-Band have been obtained.

Integrated mirrors on Si-PIC can be exploited in the up-reflecting or down-reflecting scheme accordingly to the direction of the designed steered optical beam. Two schemes for the full MOD1 MUX architecture differing in the VCSEL assembly position (top-mounted VCSEL with up-reflecting mirror and bottom-mounted VCSEL with down-reflective mirror) have been analysed. Proper sets of SOI wafers have been processed to test both configurations. In the MOD1 design up-reflecting mirrors on Si-PIC have been considered a good option to efficiently address optical beams from VCSELs into waveguides as well as to deliver optical signals toward a fiber optic assembly. Preliminary measurement results indicate a good agreement with the design targets (test performed by VTT). Mirror coupling-losses of less than 0.5 dB when interfacing with a polarization-maintaining fiber (PMF) have been obtained over the entire C-band in both TE/TM polarizations. Moreover, a set of Si-PICs with down-reflective mirrors suitable for bottom-mounted VCSEL assembly will be provided to TUE with the aim to evaluate and compare the performances. Two-stages Mach-Zehnder interferometer (MZI) for multiplexing the four sub-MOD outputs (each one equipped with 10 400-

GHz spaced VCSELs) has been designed, fabricated, and characterized in transmission in case of TE polarization. Also a phase control achieved by a heater on the longer arm of the MZI to tune the power delivered to the output port (for fiber pigtail) has been implemented. The measured transmission plots are presented in Fig. 2, while the schematic of the mask design (left) and the image of the fabricated chips (right), are shown in Fig. 3.

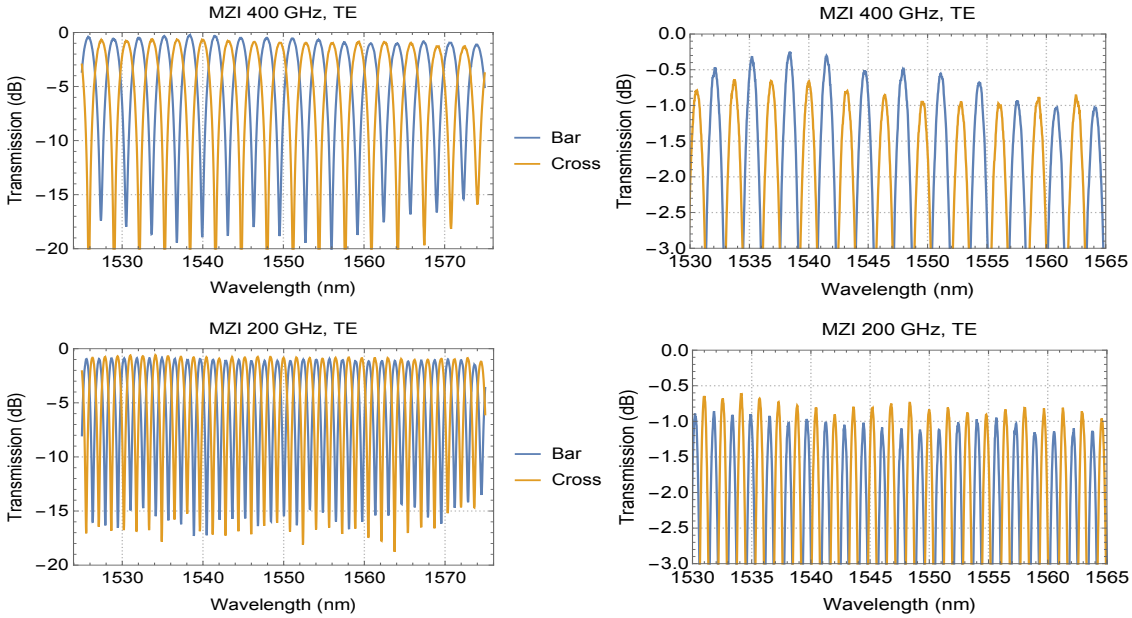

Figure 2 Measurement plots showing low insertion loss and uniformity of the performance of the MZI designs with FSR values of 400 and 200 GHz over the entire C-band.

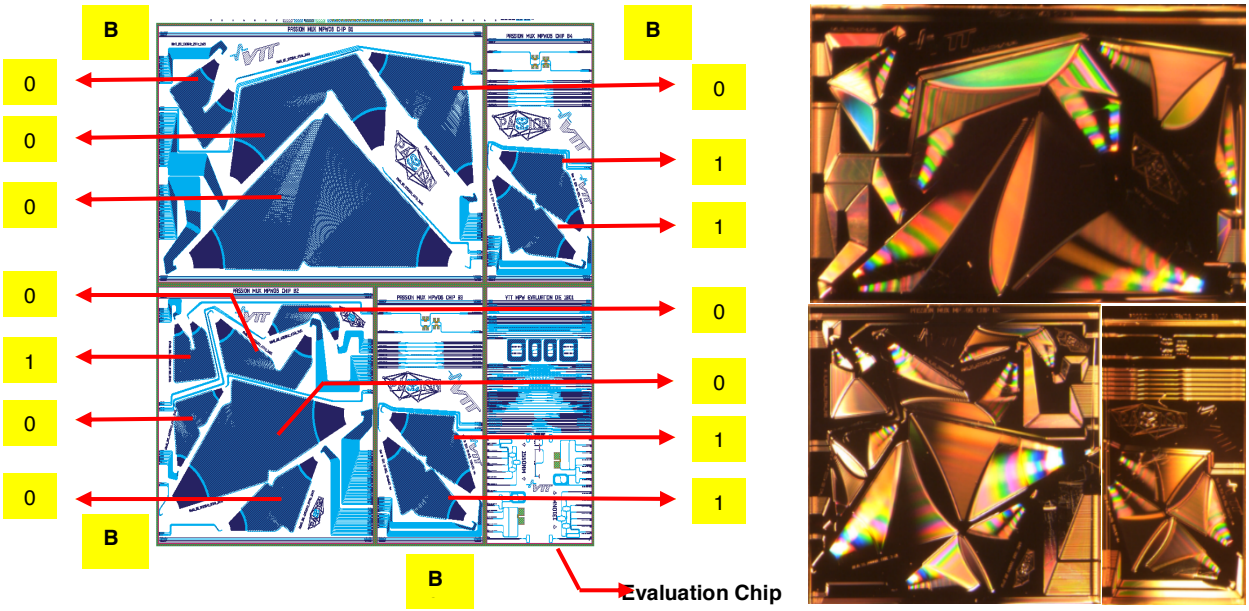

Figure 3. Mask design (left) and microscope image of the fabricated chips (right).

Initial measurements for TE polarization on an AWG design centered at ITU channel 39 (1546,12 nm) with target channel spacing of 400 GHz have shown very promising performance, such as insertion loss of about ~ 3 dB, channel spacing of ~ 395 GHz, 3-dB channel bandwidth of ~ 153 GHz, and extinction higher than 35 dB.

Similarly to AWG, also EG designs have been pursued targeting the same component specifications. Due to the diffractive nature of the EG, the channel separation is determined by the period of the grating, as well its size and the slab or "free-space" propagation. EG design has been undertaken both at VLC Photonics and VTT. The adopted approach is based on a Rowland circle. Characterization results of the fabricated devices will be compared to find the best MUX building blocks design to be used for the final Si-PIC design configuration.

To electrically interconnect the SI-PIC with the VCSEL sources, an electrical interposer based on a Land Grid Array (LGA) pads architecture has been designed to route 648 DC lines (including ground distribution, DC power supplies and digital controls) as well as 160 critical RF lines (25 GHz) for a total amount of 808 pads (Fig.4).

Thermal management design has been also critically reviewed and a metal-inserts solution (thermal interfaces as integral parts of the LGA interposer) has been preferred with respect to the thermal-vias solution previously considered and described in the deliverable D3.1. Two thermally de-coupled heatsink paths provided by such thermal interfaces have been considered. This approach in combination with a seal-ring also provides hermetic sealing of the VCSELs on the Si-PIC.

Furthermore, to initially test and characterize MOD1 (Si-PIC assembled on LGA interposer), a specific evaluation board will be designed and exploited as test vehicle before the final implementation of the MOD1 on the main PCBs of S-BVT architectures.

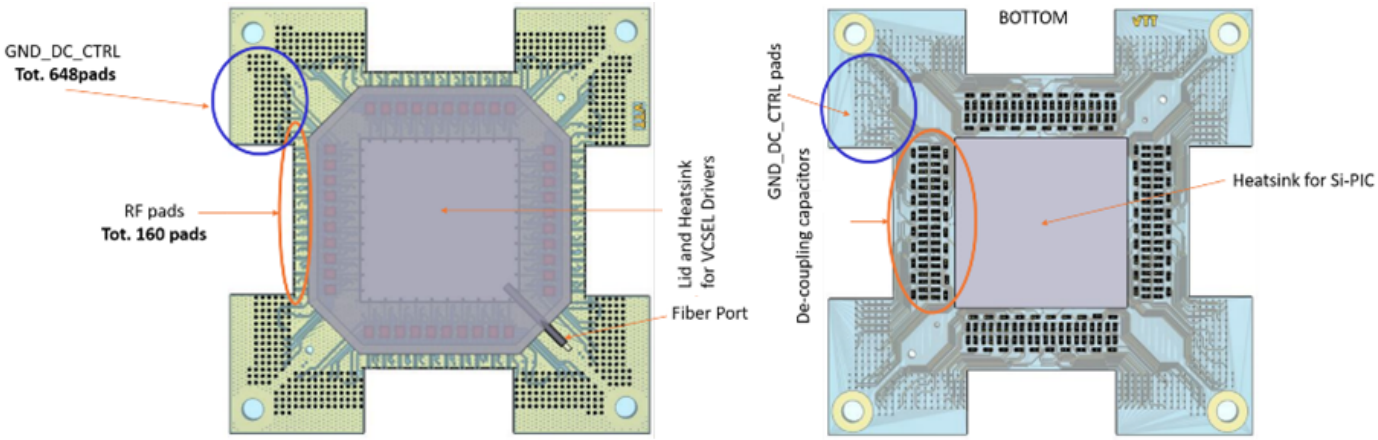

Figure 4 Land Grid Array pads architecture.