First testing of directly modulated VCSELs with selected drivers

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EXECUTIVE SUMMARY

This report provides a detailed description of the selection and of the first experimental characterization of the electronic drivers necessary to directly modulate the vertical cavity surface emitting laser (VCSEL) sources developed in the PASSION project.

The PASSION architecture, and in particular the silicon photonics chip design, the VCSEL characteristics and the preferred modulation format are taken into account to define the driver performance and dimensions necessary to fulfil PASSION targets in terms of transmitted capacity.

The selected drivers are tested by wire bonding with PASSION VCSELs with different modulation formats i.e. discrete multitone modulation (DMT), on-off keying (OOK) and 4-level pulse amplitude modulation (4-PAM).

The results obtained so far are encouraging and indicate a preferred driver both in terms of performance and power consumption.

1 INTRODUCTION

This report will provide a detailed description of the selection and of the first experimental characterization of the electronic drivers necessary to directly modulate the VCSEL sources developed in the PASSION project.
The VCSEL drivers are required for the realization of the PASSION module, which will support target capacities up to 50 Gb/s per device. Hence, the drivers must operate according to specific requirements given by:

- the VCSEL high-bandwidth modulation exploiting multi-level or multi-subcarrier modulation formats, such as multiple pulse amplitude modulation (PAM) and discrete multitone (DMT) modulation;
- the Tx architecture based on a modular approach comprising the realization of multiple VCSEL sub-modules, modules and super-modules;
- the integration of clusters of multiple VCSELs bonded and optically coupled on a Silicon-Over-Insulator (SOI) Photonics Integrated Chip (PIC) (Si-PIC), which embeds wavelength multiplexing capabilities, with the design described in the Deliverable D3.1.

To be compliant with the above conditions the VCSEL drivers employed in PASSION must satisfy strict specifications, for example in terms of:

- modulation bandwidth;
- modulation swing;
- response linearity;
- bias current level;
- bias control resolution;
- ADC bit number;
- dimensions
- power dissipation.

After the description of Tx architecture adopted in PASSION conditioning the driver choice in Section 2, we report in Section 3 the driver selection process among the commercial products available on the market, identifying the specific supplier. In Section 4 the driver samples preparation and setup are described, while finally in Section 5 the first experimental tests of the selected drivers together with VERTILAS VCSELs are presented. The results presented in this Deliverable D3.2 constitute the achievement of the Milestone M3.2 “Direct modulation of VCSELs demonstrated with selected drivers”.

2 PASSION TX ARCHITECTURE

In this Section we describe the PASSION Tx architecture in terms of design, VCSEL operation and target performances to justify the requirements required to the VCSEL drivers in order to be employed in the Tx implementation.

2.1 VCSEL SOURCES

In PASSION project, the VCSEL devices are developed and produced by the partner VERTILAS with the following targets:

- single mode operation;
- low power consumption < 35mW
- output power about 4 mW @ 20°C
- bandwidth S_{21} = 20GHz
- layout optimized for flip chip bonding
- far field FWHM < 12°
- SMSR > 35dB
- low threshold current I_{th} < 2.5 mA @ 20°C

The high modulation bandwidth (up to 20 GHz) requires to adopt a short-cavity design, achieved by means of a very short resonator length and an active region optimized for high bandwidth, as shown in Figure. 1. Such a bandwidth allows to directly modulate the VCSEL in order to achieve up to 50-Gb/s signal rate per each VCSEL, by exploiting DMT or PAM modulation (e.g. 4-PAM modulation).

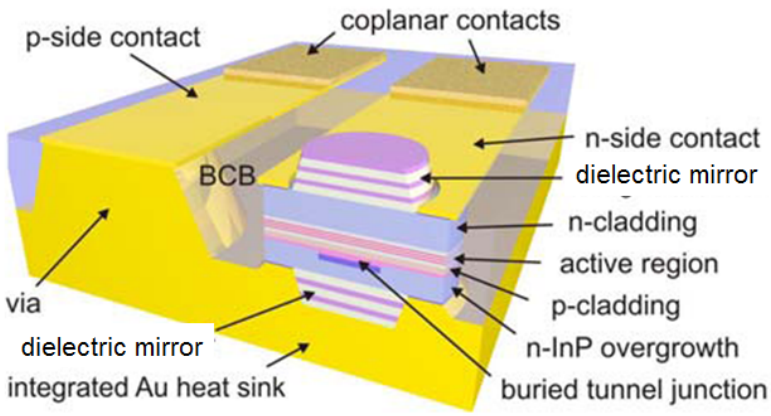

Figure 1. Cross section of the short-cavity VCSEL optimized for high modulation bandwidth.

For the realization of the PASSION Tx, VCSEL emission is required to cover the whole frequency range from 191.9 THz (corresponding to the ITU-T WDM channel CH19 at 1562.23 nm) to 195.9 THz (CH59 at 1530.33 nm). In order to provide lasers to cover this wavelength range, the laser technology needs to be based on InP material. InP wafers are the basis to grow quarternary and tertiary semiconductor layers, e.g. InGaAs, InAlAs and InGaAlAs to realize DBRs, an active region and further laser structures. The optical and thermal characteristics of this material system pose a challenge to the optical and thermal design of such a vertical surface emitting laser. Lasers require a sufficient optical power and min. bandwidth for successful high speed operation and reliability. This can only be accomplished by overcoming the limitations of the material system to realize a laser design with an optimized thermal resistance and effective optical performance. This can be achieved with a short resonator length (corresponds to photon life time) and maximized heat sinking. VERTILAS VCSEL design features both a top and bottom DBR based on dielectric material, as well as a pseudo substrate based on plated Au at the bottom of the wafer or VCSEL. The high-reflective dielectric material reduces the numbers of mirror pairs significantly, thus reducing the resonator length that corresponds directly to the photon lifetime and device bandwidth. The design enables an effective heat flow from the active region to the Au heat sink, minimizing internal heating of the device. The current confinement is realized with a Buried Tunnel Junction (BTJ) and defines the active area. This active area can be adapted to modify the near and far field characteristics of the

laser. Fig. 2 shows the BTJ-based VERTILAS VCSEL structure with an emitted circular Gaussian laser beam with about 5.5 µm diameter (expected far field 10° to 12° FWHM).

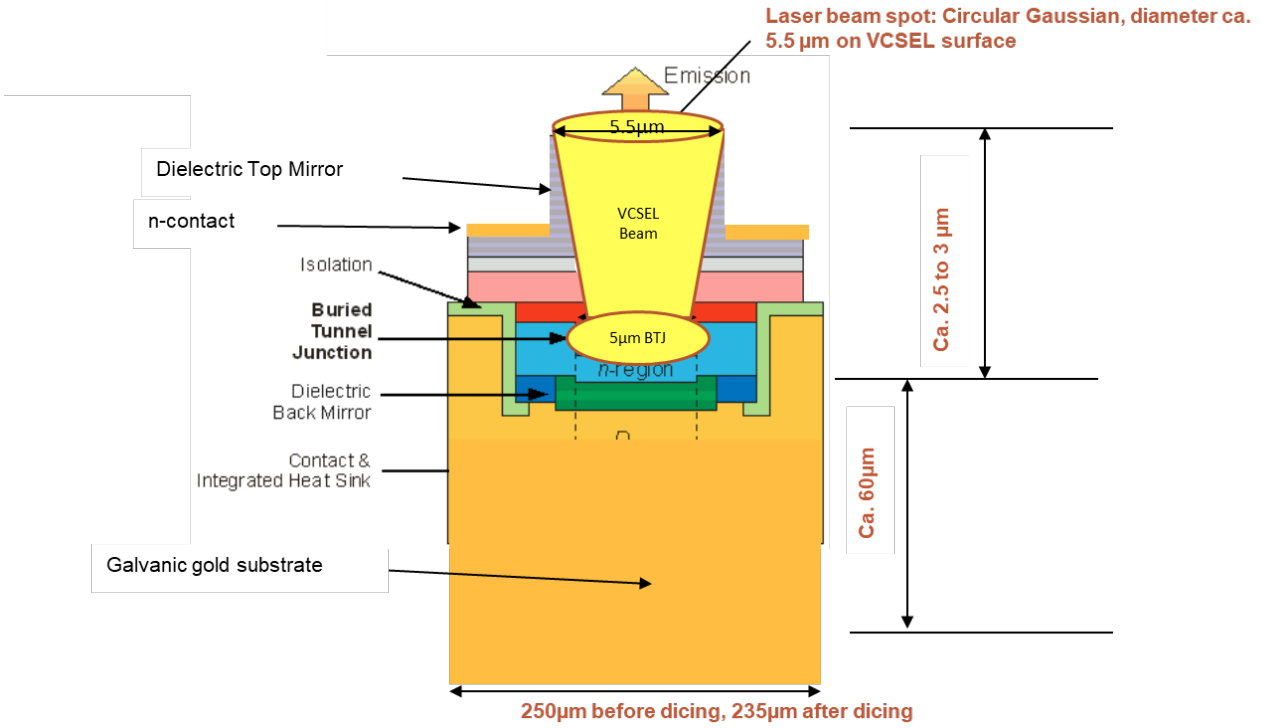

Figure 2. BTL-based VCSEL structure.

The PASSION approach requires that each VCSEL could be finely tuned in a 25-GHz channel grid to match with the design of the WDM multiplexers. To satisfy this requirement the VCSEL will be designed to target different emission wavelengths covering the C-band with 100-GHz spacing and further tuning over the 25-GHz grid will be achieved through current tuning.

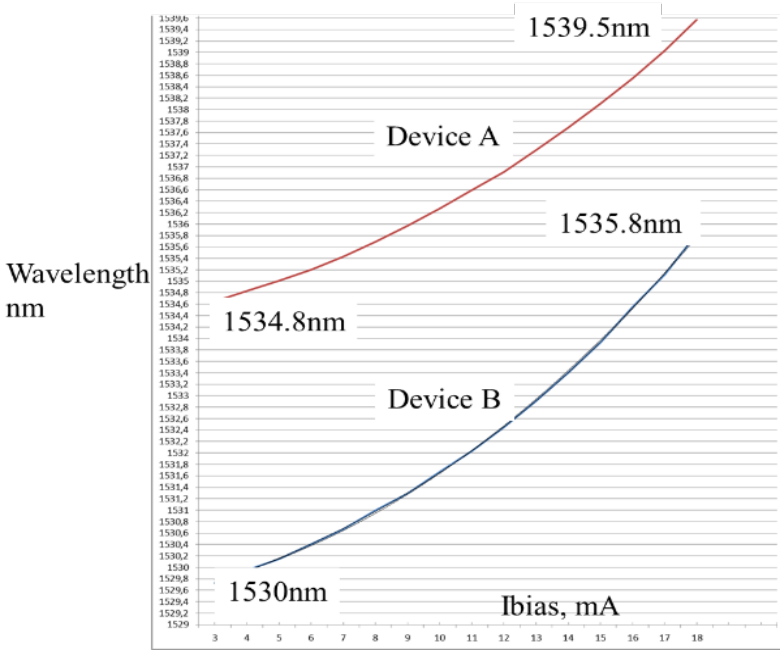

Figure 3. C-Band VCSEL emission tuning by means of the bias current.

The goal is to provide lasers covering the ITU channels 10 to 59 with an effective grid of 25 GHz. Vertilas plans to manufacture several wafers covering certain wavelength ranges. From these wafers, the VCSELs can be selected for particular ITU channels. Due to large current wavelength tunability, the VCSELs can be finely tuned by Ibias to match the narrow 25 GHz channels. This current tunability is demonstrated in Fig. 3 for two different devices A and B. During the PASSION project, new devices will be developed to cover the requested wavelengths range and improve the performance. The current tuning coefficient of the VERTILAS VCSELs is ca. 0.1/0.2 nm/mA, depending on the laser design and applied bias current. The temperature tuning coefficient is comparable to other InP based laser technologies with ca. 0.1nm/°K. Moreover, Fig. 4 shows the operation of the VERTILAS VCSEL as a function of the bias current. To exploit the full S21 bandwidth, the Ibias should satisfy the relation $\sqrt{I_{bias} - I_{th}}$)= 2.5/3 achieving the maximum modulation bandwidth.

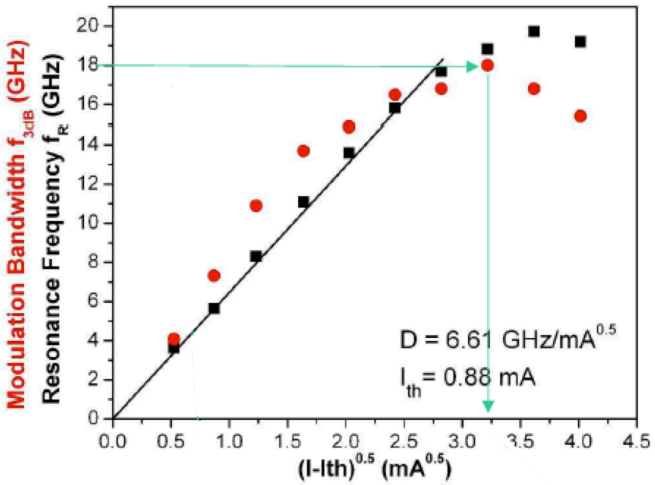

Figure 4. Modulation bandwidth (red circle) and resonance frequency (black square) as a function of the Ibias. Maximum bandwidth is achieved at I_{bias} of about 11-11.5 mA, corresponding to $(I-I_{th})^{0.5}$=3.24 (I_{th}=1 mA).

2.2 PASSION MODULAR APPROACH

One of the main objectives of PASSION project is the development and deployment of a photonic Tx to support agile metro networks, capable of enabling target capacities higher than Tb/s per spatial channel, higher than 100 Tb/s per link and Pb/s per node by means of spectral and spatial aggregation. PASSION's goal is achieved by exploiting VERTILAS VCSEL sources, described in the paragraph 2.1, each one operating at a different 25-GHz spaced WDM wavelength in the C-band, directly modulated to obtain up to 50 Gb/s rate, to target up to 8-Tb/s WDM aggregated capacity at a single polarization. 16 Tb/s per spatial channel are achieved exploiting polarization-division multiplexing, while the spatial dimension of 7 cores MCF or 7 fibers in a bundle allows enabling up to 112 Tb/s aggregated capacity per link.
This objective is pursued with a modular approach as shown in Figure 5. A 40-VCSEL based module is built by integrating 4 sub-modules, each one containing 10 VCSELs. The 40 emission wavelengths cover the entire C-band with 100 GHz granularity and are fine-tuned in a range of 0-75-GHz through the VCSEL bias current and stabilized by a temperature cooler. By 50-Gb/s modulation of each VCSEL, an aggregated capacity of 2 Tb/s per module is achieved. By combining four of such a module with external inter-leavers a full 160-ch Tx super-module (characterized by 8 Tb/s capacity) is obtained with 25-GHz wavelength granularity. This type of modularity offers the ability to fabricate

and stock only one module type, and to use the identical 40-ch modules to build the full 160-ch Tx super-module. Then, a discrete polarization multiplexer combines inputs from two identical 160-ch Tx super-modules to get 16 Tb/s capacity. Finally, signals are coupled to multi-core fibers or fiber ribbons using spatial multiplexers for the fully equipped S-BVT (112-Tb/s in capacity).

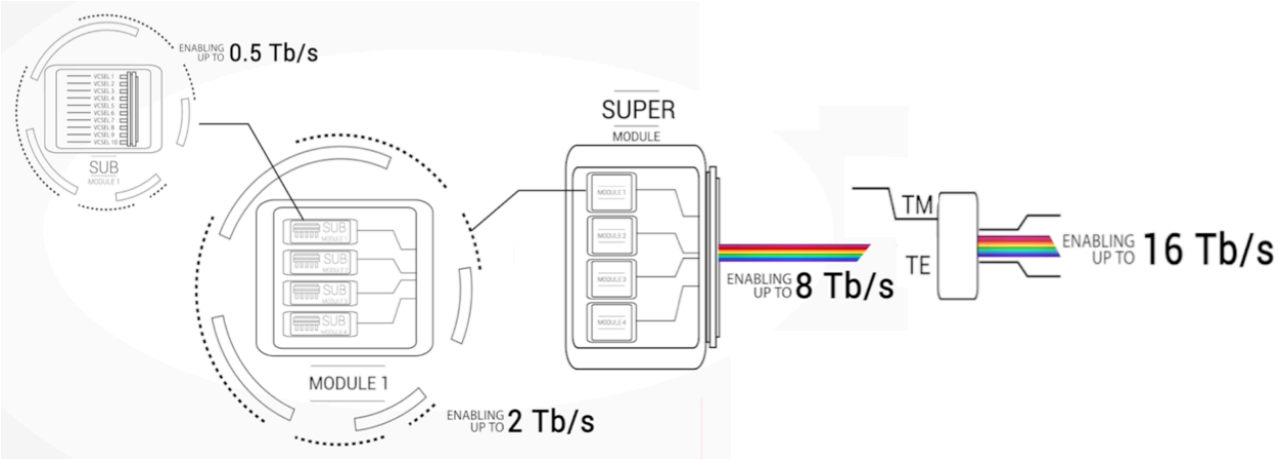

Figure 5. Example of Tx module capacity aggregation exploiting the spectral and space dimensions.

2.3 SILICON PHOTONICS CHIP DESIGN

The module structure representing the smallest discrete granularity element in PASSION aggregation modular approach is shown in Figure. 6. The structure includes:

- 1 x SOI PIC embedding 40 channels (100-GHz spaced), 4 x10 input channels (400GHz spaced) optical multiplexers (MUX#1-4) having their respective outputs furthermore multiplexed into MUX#5 whose output represents the exit port to couple light into a pigtailed single mode polarization-maintaining fibre (PMF) assembly.
- 40 x VCSEL chips (directly modulated up to 50Gb/s each)
- 40 x linear VCSEL driver chips
- 1 x Land Grid Array (LGA) redistribution layers (RDL) fan-out electrical interposer, embedding 2 differentiated thermal sinking paths able to separate heat flows generated by VCSELs (which require an active cooling set a 40°C ± 0.1°C) from the thermal payload generated by linear drivers (which can be passively dissipated in air with a standard heat sink design).

As reported in the Deliverable D3.1, VCSEL drivers are put outside the Si-PIC chip for thermal reasons, but still at very short distance allowing wire bonds (WBs) to provide interconnections, as shown in Figure. 7 left. However, for high-speed and high bandwidth operations WBs have to be as short as possible (preferably <200μm). VCSELs are positioned as close to the Si-PIC chip edge as possible. The chosen solution is to place the 40 VCSELs, (which correspond to the 40-channels requirement of the Si-PIC chip), close to the perimeter of the SiPh chip with 10 VCSELs on each edge, as shown in Figure. 7 right.

With this architecture, the channel pitch, which is the physical spacing between the adjacent channels on any given edge of the chip, influences the chip size. In fact, the channel pitch is dependent on the pitch among the following elements: the multiplexer input arms, the VCSELs, and the drivers. Consequently, the maxima of these elements decide the final pitch. We need thus VCSEL driver dimension to not exceed the range of 1.5-2 mm. In this way the channel pitch value of

2 mm will be obtained, taking into consideration that some additional space is needed for the output fibre placement, the chip size should be expected to be around 20 x 20 mm^2.

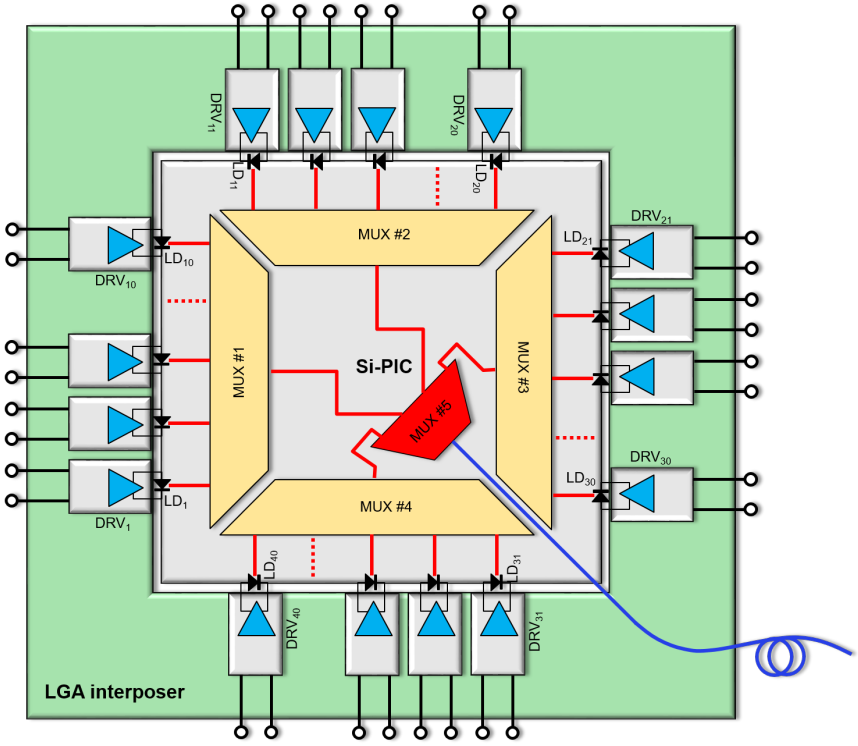

Figure 6. 40-VCSEL module structure.

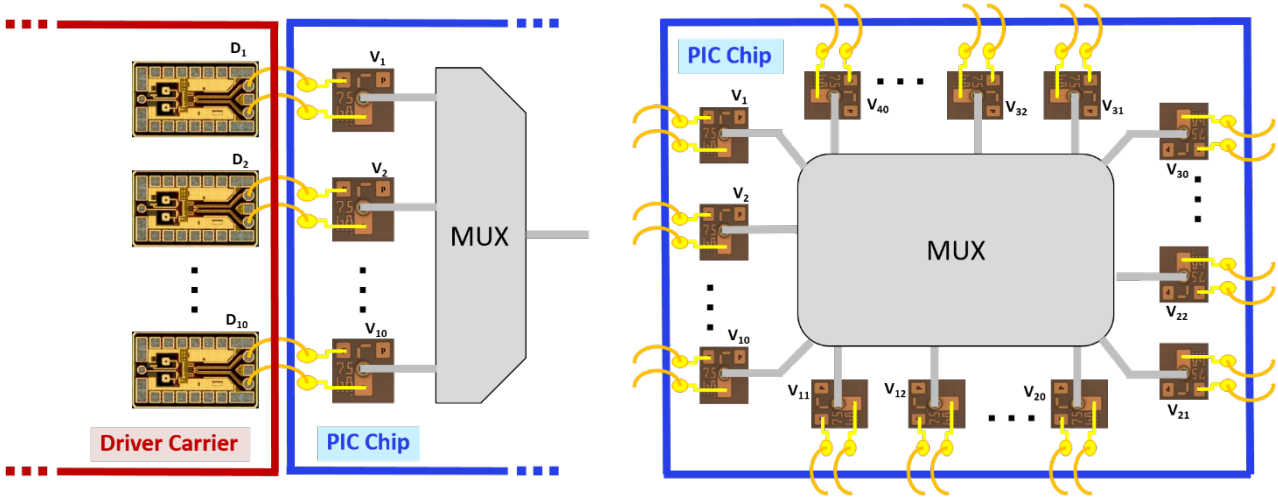

Figure 7. Module integration scheme: integration of VCSELs and drivers (left). Designed VCSEL arrangement on a 20x20 mm^2 PIC chip (right).

2.4 VCSEL MODULATION FORMATS FOR HIGH CAPACITY

Advanced modulation formats are proposed in order to exploit limited bandwidth devices (such as directly modulated VCSELs) to support PASSION expected transmission capacities [1]. In particular, multicarrier modulation, as DMT, can enable spectral manipulation leading to an efficient usage of the bandwidth resource. Furthermore, thanks to bit and power loading techniques, dynamic and flexible adaptation to traffic/channel conditions can be reached. The idea behind DMT is the partitioning of the available bandwidth into frequency sub-bands, or bins, and assigning a low baud rate modulated carrier to each bin center. The rationale is that over the sub-band bandwidth, the channel looks relatively benign and hence will require minimal equalization, which in turn simplifies implementation. This frequency bin approach is a natural for modulation by the inverse FFT and demodulation by the FFT, which gives rise to a particular subset of DMT. On the other hand, contrary to on-off keying (OOK), the exploitation of DMT requires the use of linear analog amplifiers, as for m-PAM modulation. Moreover due to the potentially large peak to average power ratio (PAPR) the amplifier should have sufficient dynamic range to handle the average signal level and signal peak amplitude without clipping or compressing [2]. These represent challenging constraints for laser driver amplifiers mainly designed so far in optical communications for OOK.

3 VCSEL DRIVER SELECTION

3.1 VCSEL DRIVER REQUIREMENTS FOR PASSION TX IMPLEMENTATION

Taking into account the Tx architecture described in the Section 2 in terms of VCSEL operation, capacity target, 40-VCSEL module design and Si integration, we can deduce the requirements necessary for the VCSEL drivers in order to implement the PASSION transceiver.

- *Modulation bandwidth: > 20 GHz*. In order to achieve up to 50-Gb/s signal rate per each channel, the VCSEL has to be directly modulated with a baudrate of around 20-25 Gbaud (PAM) or by exploiting multicarrier modulation format such as DMT over up to 20 GHz.
- *Bias current: 9-11 mA*. Considering the typical electro-optical characteristics of the short-cavity VERTILAS VCSELs, this bias current is necessary to obtain an acceptable trade-off between optical power performance and modulation bandwidth. Currently 28-Gbaud VCSEL drivers available on the market show a maximum bias current around 10 mA.
- *Resolution in the bias current control*: 1 mA. The modular approach adopted in PASSION requires that the emission wavelength of each VCSEL is finely tuned in a range of 75 GHz through the bias current. The typical tuning coefficient of the VERTILAS VCSELs is 0.1/0.2 nm/mA. This translates in the necessity to have drivers' DACs with a high number of bits (e.g. > 8 bit) depending also on the maximum bias current range.
- *Low jitter*. Total jitter for 4-PAM modulation < 12 ps
- *Linear response*. The exploitation of multicarrier modulation formats such as DMT requires a more linear response of the driver than in case of standard OOK modulation and similar to M-PAM modulation needs.
- *Dimension: < 2 mm*. In the design of the integrated 40-VCSEL module, the driver dimension decides the pitch between adjacent elements (VCSEL + driver + multiplexer input arm), conditioning the final chip size. The target is to maintain the 40-VCSEL module size in 20x20 mm^2.

- *Low power dissipation: < 400 mW*. One of the PASSION goal is to reduce the power consumption of the whole system. VCSELs guarantee energy-saving operation. Also the driver has to maintain low its power dissipation.
- *Chip internal temperature measurement and remote control of driving parameters*. Required features for the VCSEL driver include a number of integrated programmable functions such as the chip internal temperature measurement, as well as a serial peripheral interface or I^2C bus controller to set and remotely control all optimal working driving parameters for each single VCSEL chip.

3.2 MARKET SURVEY

A market survey has been performed to identify a suitable driver which can guarantee the requirements described in the paragraph 3.1 and necessary for the implementation of the PASSION Tx. The survey was focused not only on drivers for VCSELs, but also on drivers finalized for direct modulated laser (DML) and electro-absorption modulated laser (EML) modulation, in order to provide the bias current levels required in PASSION applications. In particular, among all the commercial drivers available on the market considered in our survey, we analysed:

- MACOM MO2170 11.3-Gbps DML driver
- MACOM MO2171 11.3-Gbps VCSEL driver
- MACOM MO2172 11.3-Gbps EML driver
- MACOM MALD-37030A 28-Gbps laser driver
- MACOM MALD-37031A 28-Gbps laser driver
- IDT HXT14100 VCSEL 28-Gbaud/s driver
- IDT HXT44100 DML 28-Gbaud/s driver

Two possible candidates for PASSION Tx implementation have been selected among the list above and mainly for the required linearity we had to discard digital drivers; the selected drivers produced by IDT – Integrated Device Technology, are described in the following paragraph 3.3.

3.3 SELECTED DRIVERS

From our market survey we selected two possible IDT drivers able to match the PASSION requirements: HXT14100 VCSEL driver and HXT44100 DML driver. Both of them support 56-Gb/s rate by exploiting 4-PAM format, so assuring high bandwidth and linearity. VCSEL driver guarantees lower power consumption, but its maximum bias current is about 12 mA, so its effectiveness in the modulation of the VERTILAS VCSELs has to be experimentally verified. The detailed description of their characteristics is presented below.

3.3.1 IDT HXT14100 VCSEL driver

HXT14100 is a single channel, low power, linear PAM4 VCSEL driver for SR optical applications that supports signalling rates up to 28GBuad or 56Gbps 4-PAM. In conjunction with an individual laser source, the device handles the complete digital-to-optical conversion, including CML input with equalization, laser driver, drive control and supervision. HXT14100 also integrates a number of functions required for Automatic Power Control (APC), as well as internal and module temperature measurements and reporting. Using the included RSSI input, the module received

optical power can also be measured. It is designed for direct DC-coupled die in TOSA applications with a small number of additional components for cost-effective and compact assemblies. HXT14100 typical applications are SFP56 Ethernet modules for datacentre applications, 50G Ethernet SR AOC, Fiber Channel modules, Infiniband EDR optical modules. In the following the features of HXT14100 VCSEL driver are detailed:

- 230mW per channel power dissipation typical
- Supports up to: I_{MOD} = 12mA$_{PP}$ and I_{bias} = 12mA with V_{CC} = 3.3V
- Integrated 12-bit ADC with 6 channel analog multiplexor front-end
- Programmable 8-bit Laser Modulation and Bias current control
- Integrated Bias Monitor, Transmit and Receive Power monitor capability
- APC
- Programmable Input LOS and Squelch function with disable, Transmit Disable, and Transmit Fault indication
- Programmable Input CTLE Equalization
- Integrated Temperature Sensor and input for external module temperature sensor
- Interrupts with User selectable Mask control
- Input Polarity Inversion
- Laser Disable for I_{MOD} and I_{bias}
- Integrated OTP for calibration
- 2-wire interface control n the current scheme of things, VCSEL drivers (for thermal reasons) are expected to be outside the Si-PIC chip
- temperature range of operation: -5°C to +95°C.

The dimensions of the driver are 1350 x 1120 μm (bare die). Figure 8 reports the HXT14100 functional block diagram.

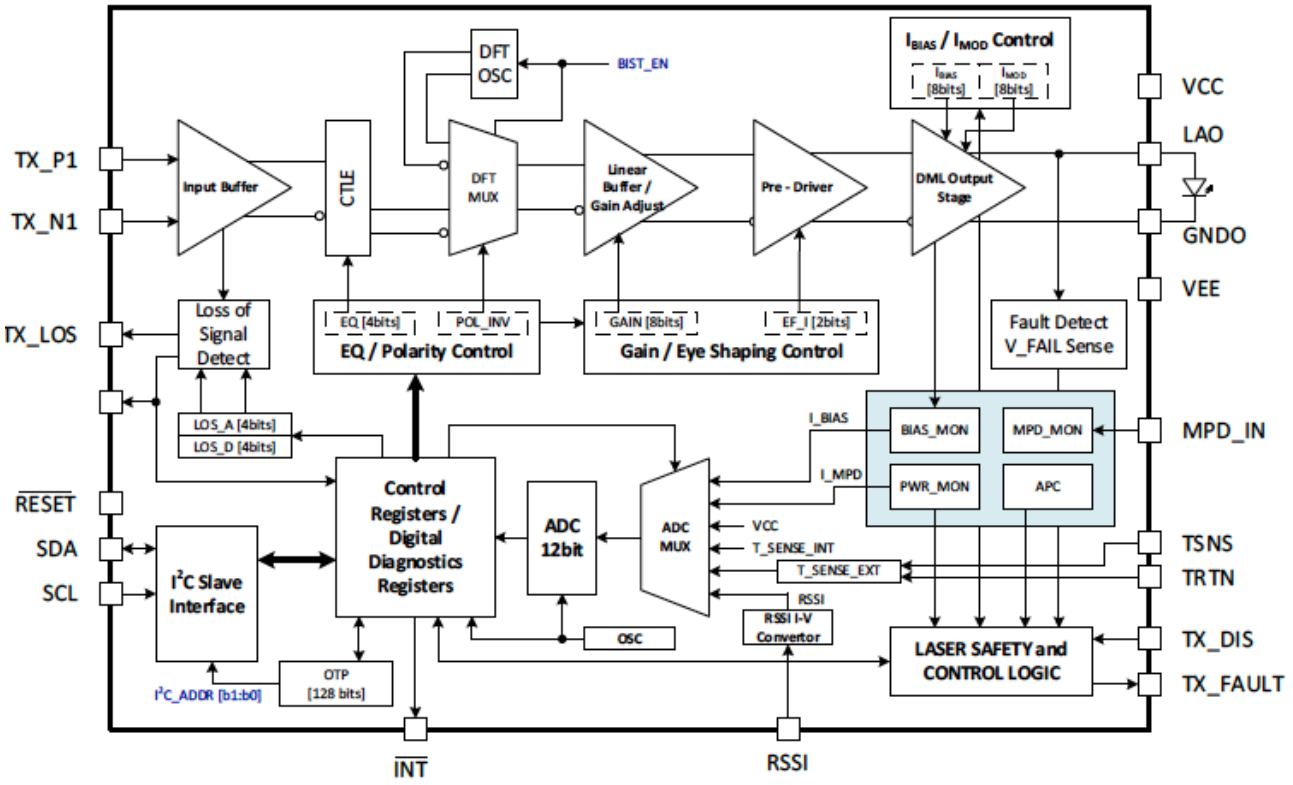

Figure 8. Functional black diagram of the HXT14100 driver.

3.3.2 IDT HXT44100 VCSEL driver

HXT44100 is a single channel, low power, linear PAM4 DML driver for SR optical applications that supports signalling rates up to 28GBuad or 56Gbps PAM4. In conjunction with an individual laser source, the device handles the complete digital-to-optical conversion, including CML input with equalization, laser driver, drive control and supervision, power control and supervision. HXT44100 also integrates a number of functions required for Automatic Power Control (APC), as well as internal and module temperature measurements and reporting. With an additional RSSI input, one can directly measure the module receive optical power and report it. HXT44100 is designed as a directly DC-coupled die used in a TOSA application. Thus, one can reduce the number of discrete components for better RF performance, cost-effective and compact assemblies. Its applications are up to 10km Ethernet SFP56 modules for datacentre applications, Fiber Channel Modules, Infiniband EDR optical modules.

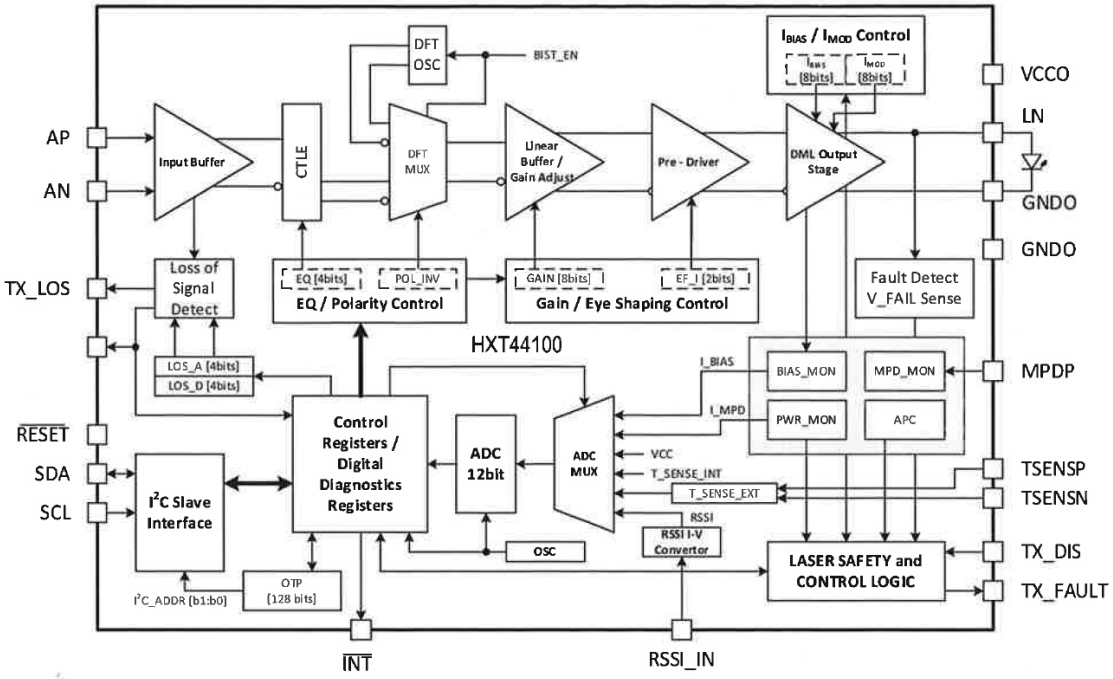

Figure 9. Functional black diagram of the HXT44100 driver.

In the following the features of HXT44100 VCSEL driver are detailed:

- 410mW maximum power dissipation per channel
- Supports up to: I_{MOD} = 60mA$_{PP}$ & I_{bias} = 60mA with V_{CC} = 2.7V
- Integrated 12-bit ADC with 6 channel analog multiplexor front-end
- Programmable 8-bit laser modulation and bias current control
- Integrated bias monitor, transmit and receive power monitor capability
- Automatic power control (APC)
- Programmable input LOS and Squelch function with disable, transmit disable, and transmit fault indication
- Programmable input CTLE
- Integrated temperature sensor and input for external module temperature sensor
- Interrupts with user selectable mask control
- Input polarity inversion

- Laser disable for I_{MOD} and I_{bias}
- Integrated OTP for calibration
- 2-wire interface control
- temperature range of operation: -5°C to +95°C.

The nominal die cut size of the driver is 1350 x 1120 μm. Figure 9 reports the HXT44100 functional block diagram.

4 EXPERIMENTAL CHARACTERIZATION SET-UP

The experimental characterization of the VCSELs with the selected drivers has required to exploit suitable evaluation boards provided by IDT for the two different models for drivers under test. The drivers and the VERTILAS VCSELs were then bonded for the testing in laboratory.

4.1 EVALUATION BOARDS

One sample of HXT14100 and one sample of HXT44100 drivers have been bonded to the respective evaluation boards. The boards need 3V voltage supply, they have differential inputs with GPPO female connectors for the RF signal (V_{pp} < 250 mV) and their operation is allowed through a graphic unit interface (GUI). Setting the GUI parameters main features of the drivers can be defined, including the bias current through BA parameter, the modulation depth through BM parameter and the equalization enabling EQEN (the gain coefficient is controlled with EQ1A1 bits). See Figures 10 and 11.

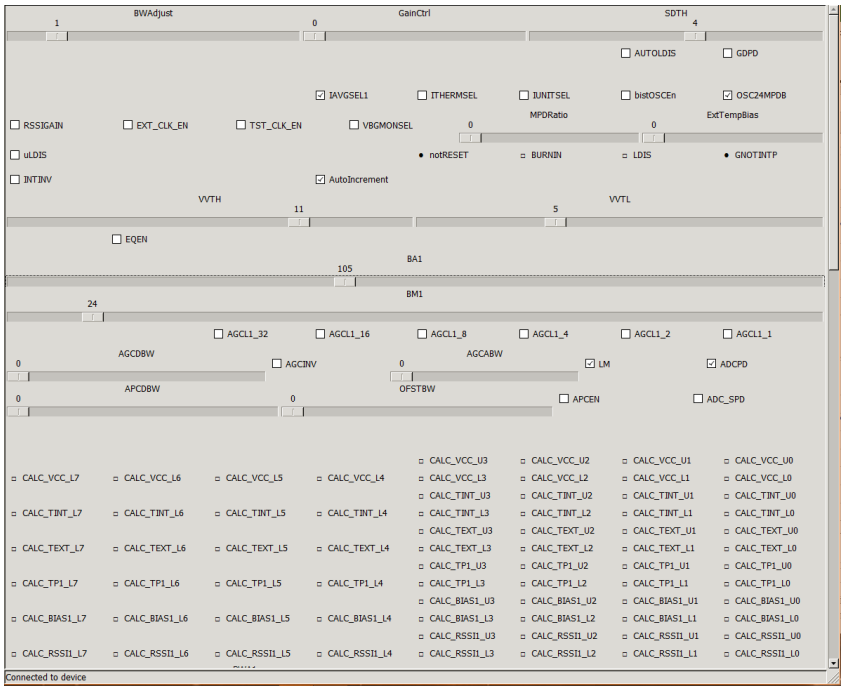

Figure 10. GUI screenshot and driver parameters - 1.

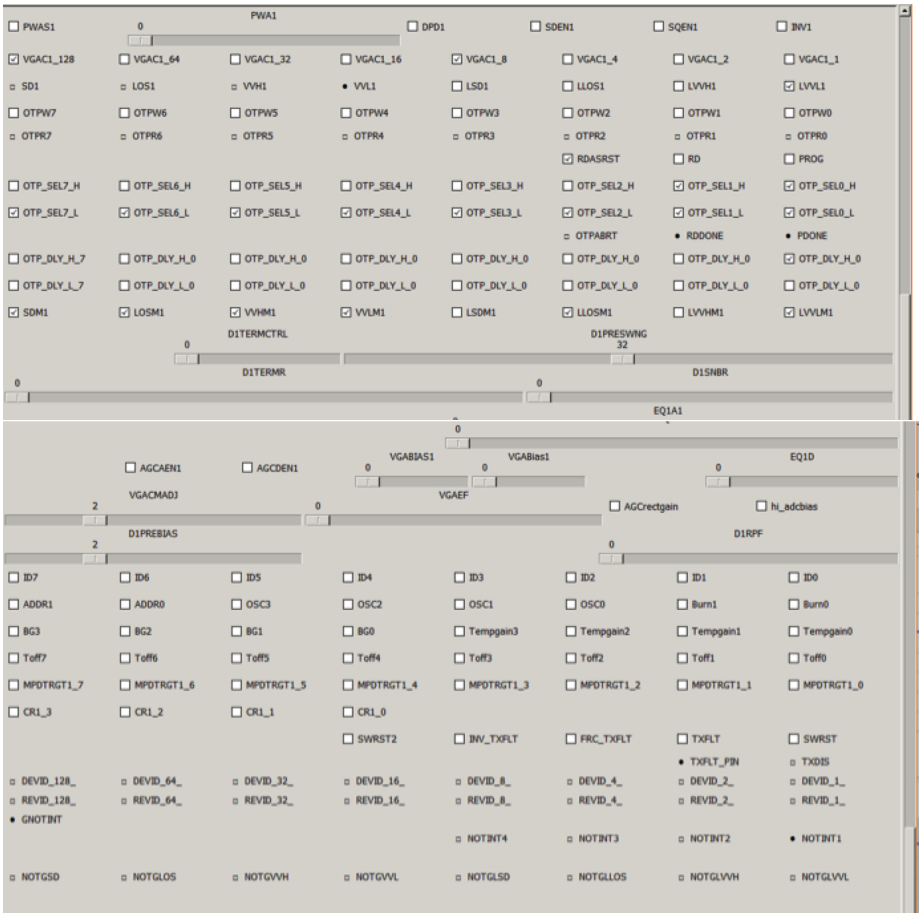

Figure 11. GUI screenshot and driver parameter - 2.

4.2 VCSEL WIRE BONDING

The IDT driver evaluation board already featured a mounted and wire bonded laser driver. Vertilas now die mounted the VCSEL device as close as possible to the driver chip. The area around the driver is metallized and connected to GND. Due to the polarity of the Vertilas VCSEL, the bottom of the chip represents the anode. The laser driver has a positive voltage on the output stage. So this requires to wire bond the GND output of the driver output stage to the top cathode (n) contact pad of the VCSEL and the signal output to the top anode (p) contact pad of the chip. The top anode contact is connected to the bottom of the VCSEL chip by a Au via structure. The VCSEL chip needed to be mounted on an isolating carrier to prevent that the GND contact of the eval board is electrically connected to the VCSEL anode. In order to keep the height difference between laser driver and VCSEL to a min., a ceramic carrier with 100μm thickness has been chosen. The wire bonding from the laser driver output stage to the VCSEL poses a challenge due to the small contact pads. Wedge-wedge bonding did not work. Therefore a 17μm Au wire with a ball-wedge bonding tool has been deployed. The following picture shows the VCSEL chip and the two wire bonds from the driver to the laser. Due to the layout of the evaluation board and positioning of the driver chip, the wire bonds are relatively long and will pose a limitation on the RF performance. This needs to be optimized for the PASSION design.

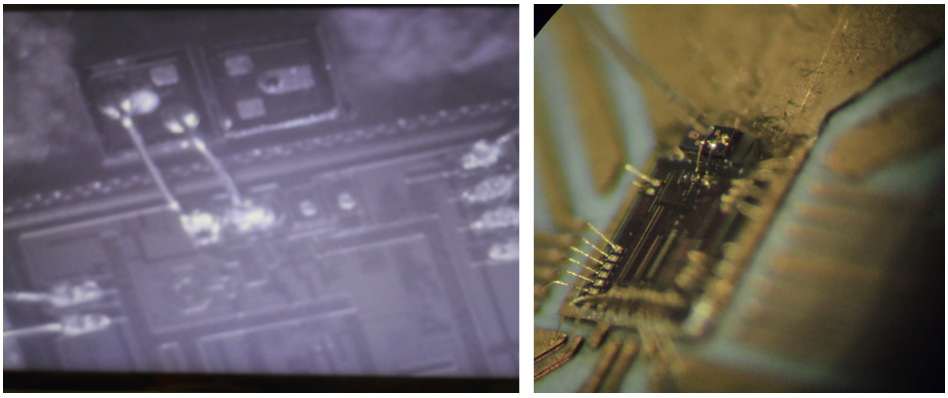

Figure 12. Close up of the VCSEL bonding.

4.3 EXPERIMENTAL SETUP

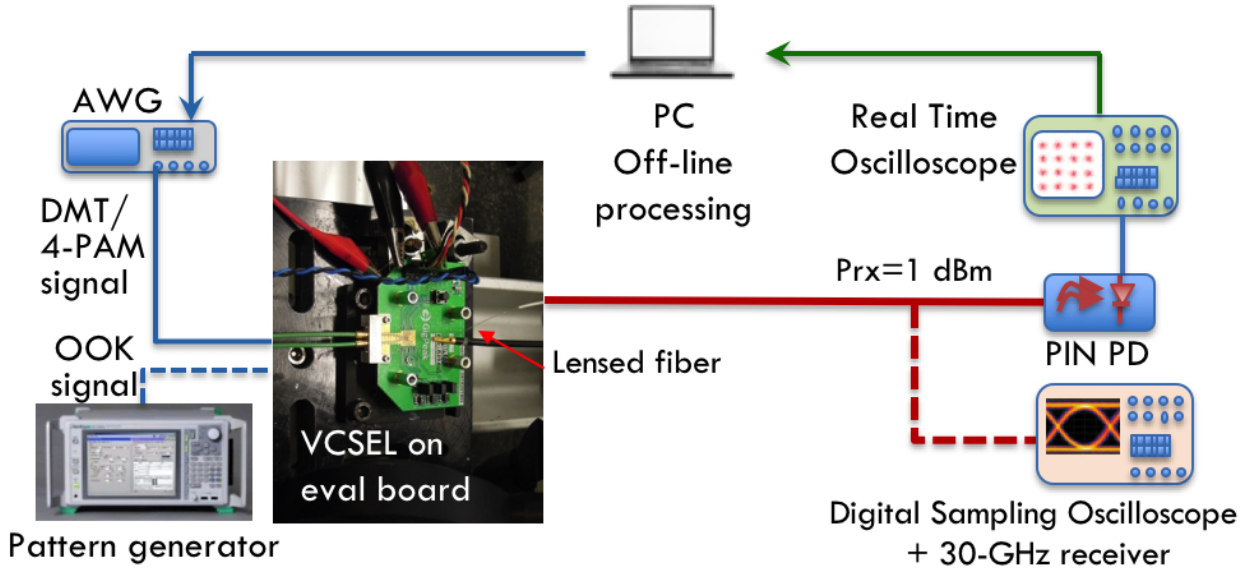

Figure 13. Setup for performance evaluation of the combination of VCSEL and HTX drivers

The two VCSELs bonded with HXT14100 and HXT44100 drivers respectively were optically coupled with a lensed fibre (see Figure 13) in order to perform the performance evaluation. The RF driving signal directly modulates the VCSELs and is generated by a Tektronix 50 GS/s arbitrary-waveform-generator (AWG 70001A) with 14-GHz electrical bandwidth for DMT and 4-PAM modulations or by a 12.5 Gb/s Anritsu or a 25 Gb/s Centellax pattern generator for OOK modulation. At the receiver side we exploited a 14-GHz or a 20-GHz PIN photo diode (PD) connected to a Tektronix real-time oscilloscope (DPO 73304DX) with 8 bits vertical resolution, 50 GS/s and 33-GHz electrical bandwidth; alternatively a Tektronix digital sampling oscilloscope (DSO) was used with a 30-GHz optical probe to display the eye diagrams; the received power was kept at 5 dBm and 0 dBm for PIN exploitation respectively and around 5 dBm for the optical probe use. In particular the DMT signal is calculated by Matlab® and is composed by 256 sub-carriers in 16 GHz range for signal to noise ratio (SNR) evaluation and in 10 GHz range for capacity performance evaluation (Chow's algorithm, is employed for bit- and power-loading [3] with a target BER of 3.6 10^{-3} as for standard 7% overhead FEC), while a cyclic prefix (CP) of about 2.1% of the symbol length is added. After A/D conversion

operated by the DPO the off-line processing provides digital symbol synchronization, CP removal, sub-carriers phase recovery, demodulation and BER count.

5 EXPERIMENTAL TESTING OF THE VCSELS WITH THE SELECTED DRIVERS

5.1 IDT HXT14100 DRIVER TESTS

The HXT14100 driver is specifically target for the employment with VCSELs thus is able to provide maximum bias and modulation currents typical for these devices.

5.1.1 CW characterization

At first we measured the power versus current curve (see Figure 14) obtained by monitoring the bias current monitor pad of the evaluation board. We then set as follows, the GUI parameters to obtain a bias current around 13 mA and a maximum modulation current of 11 mA: BA=105, BM=24, DTERM=15; VGAC=99.

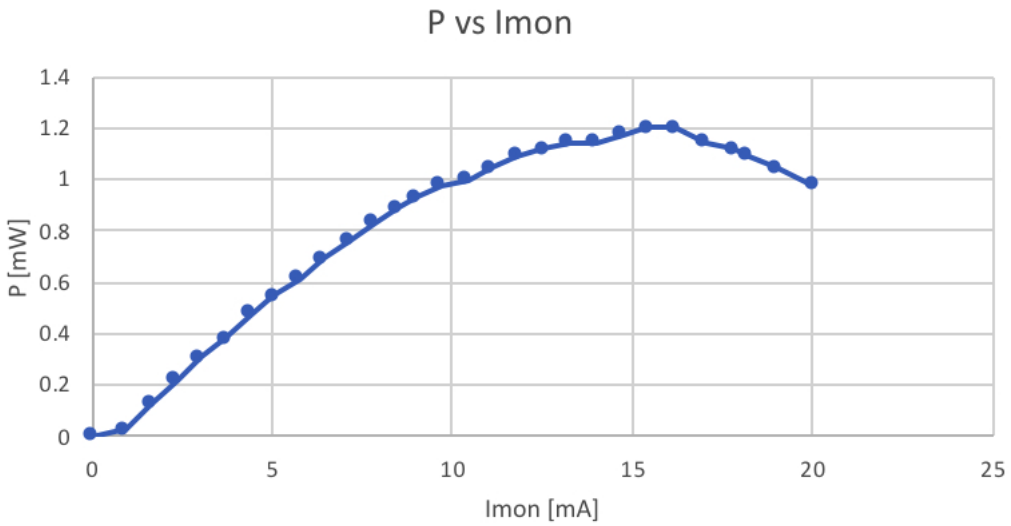

Figure 14. VCSEL output power as a function of the bias current.

Figure 15 presents the VCSEL spectra in CW mode with Ibias of 13 mA and under DMT modulation.

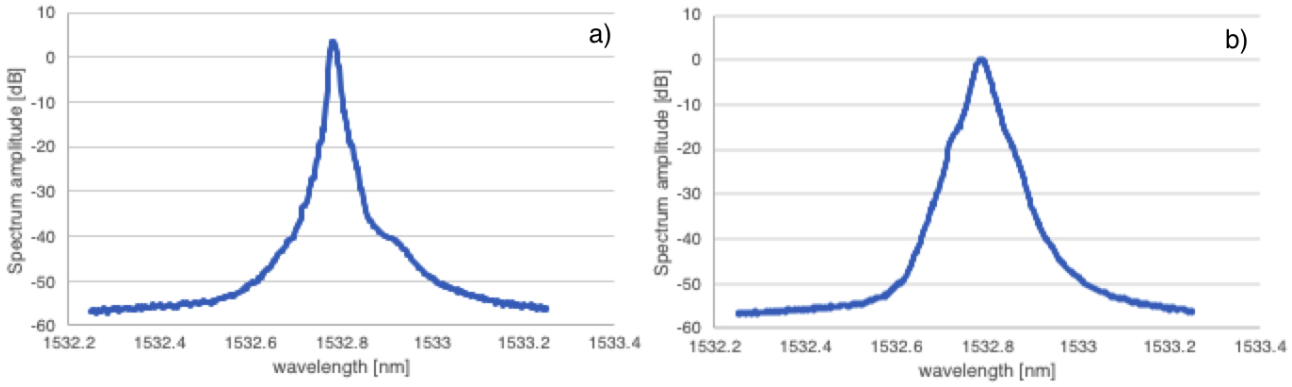

Figure 15. VCSEL optical spectrum: a) CW mode with Ibias=13mA; b) under DMT modulation with 11 mA peak-to-peak modulation depth.

5.1.2 DMT modulation with 16-GHz bandwidth

By transmitting a probe DMT signal, mapped with uniform QPSK loading over 16-GHz bandwidth we measured the SNR of each sub-carrier after direct detection (employing the 25-GHz PIN PD). The SNR curves displayed in Figure 16 represent the transmitter-receiver chain transfer functions: in blue without equalization and in red with the HXT14100 equalizer on. As can be seen (blue curve) the chain presents a decrease with a slope around 1dB/GHz, actually limiting the bandwidth below the expected values due to drivers, VCSELs, and AWG (supposed >14GHz). We suppose that this limitation could arise from the wire bonding between laser driver and VCSEL (see 4.2). The root cause for this limitation will be evaluated by performing further wire bonding and layout tests. The equalization partially overcomes this supposed limitation, still the 14-GHz step due to the AWG bandwidth limitation can be seen.

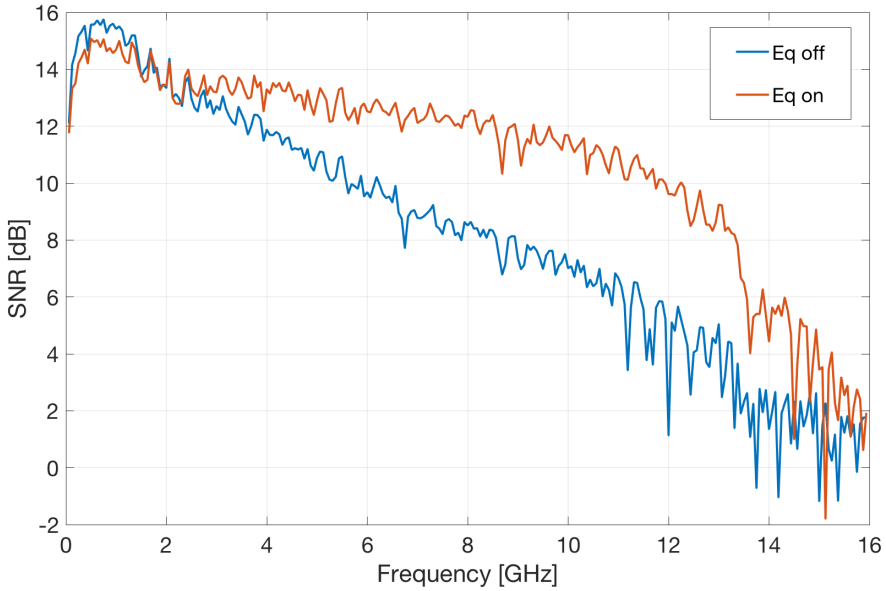

Figure 16. SNR vs subcarriers/ frequency

5.1.3 DMT modulation for transport capacity performance evaluation

It is envisaged that, to achieve PASSION target transported capacities, either dual sideband (DSB) or single sideband (SSB) DMT modulation will be used. In this preliminary study we focus on DSB DMT which, in order to match the 25-GHz optical channel grid, is allowed to occupy a maximum electrical spectrum of 12.5 GHz [4]. In order to provide a guard-band we start with covering a 10-GHz bandwidth, which will be further optimized during the project.

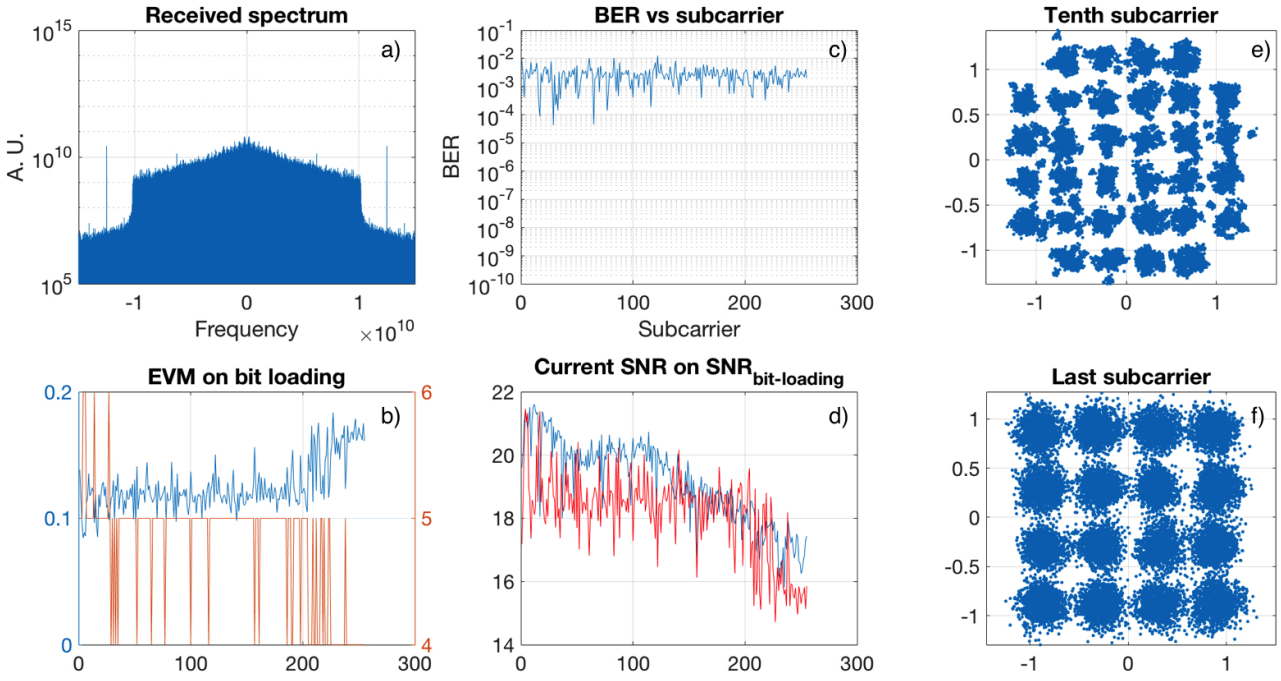

Figure 17. DSB DMT transmission over 10-GHz electrical spectrum, driver equalizer off: a) electrical spectrum vs frequency; b) EVM (blue) and bit loading (red) vs subcarrier number c) BER vs subcarrier number; d) actual (blue) and bit-loading equivalent (red) SNR vs subcarrier number; e) tenth subcarrier constellation diagram; f) last subcarrier constellation diagram.

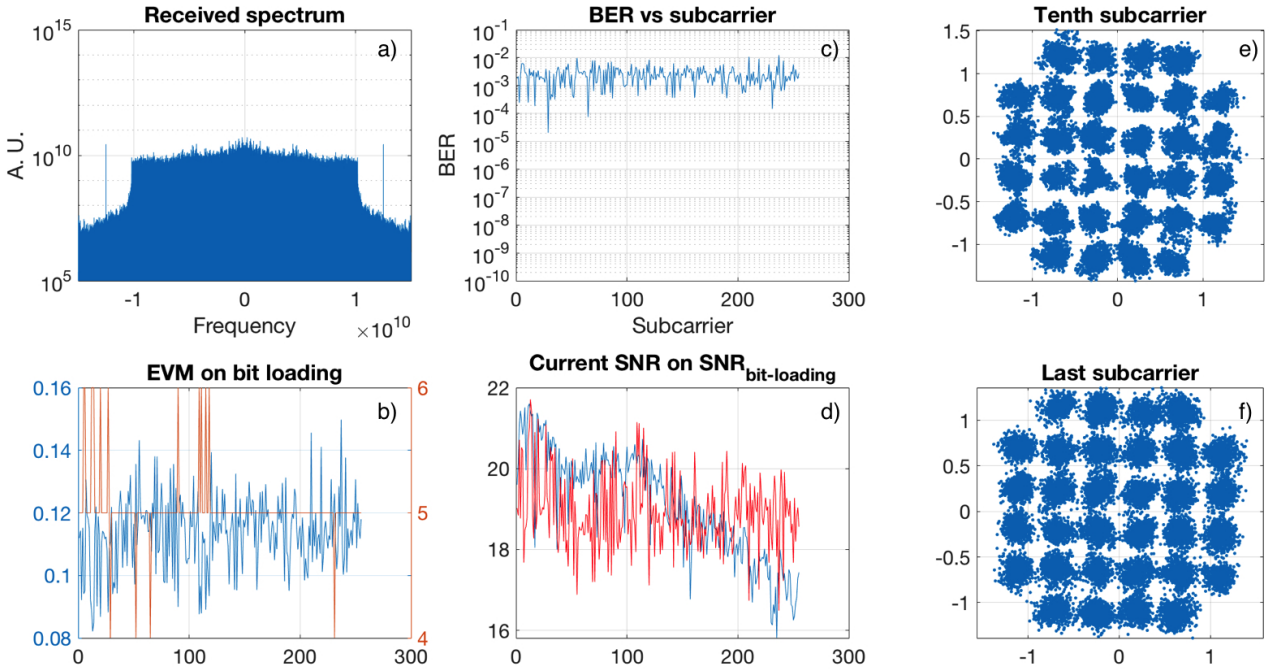

Figure 18. DSB DMT transmission over 10-GHz electrical spectrum, driver equalizer on: a) electrical spectrum vs frequency; b) EVM (blue) and bit loading (red) vs subcarrier number; c) BER vs subcarrier number; d) actual (blue) and bit-loading equivalent (red) SNR vs subcarrier number; e) tenth subcarrier constellation diagram; f) last subcarrier constellation diagram.

The results obtained disabling or enabling the driver equalizer are displayed in Figures 17 and 18 respectively. As can be seen by comparing the two spectra (Figure17a) and Figure 17b)) the equalizer correctly acts on higher frequencies, actually allowing a higher SNR and thus to exploit higher modulation formats in subcarriers with a high number; for example, the last subcarrier moves from 16 QAM (Figure 17e) to 32 QAM (Figure 18e). The overall supported capacities are 48.7 Gb/s and 50.2 Gb/s respectively.

5.1.4 OOK modulation

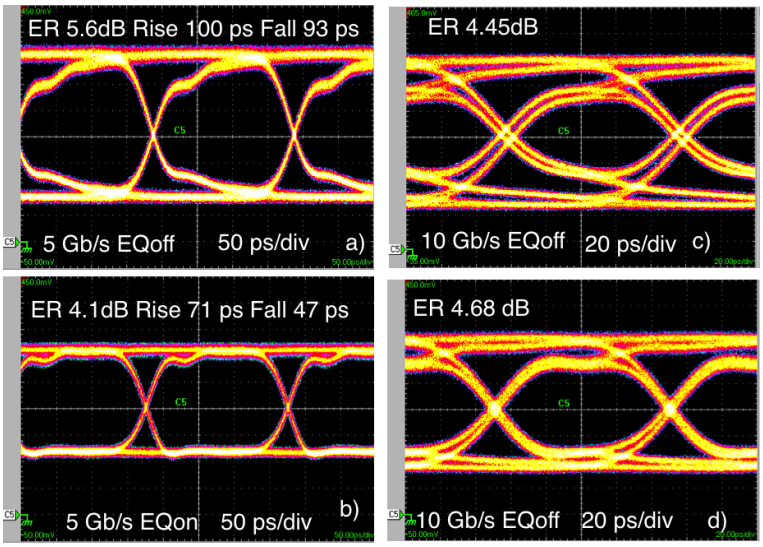

Figure 19. OOK eye diagrams: a)5 Gb/s equalizer off; b) 5 Gb/s equalizer on; c) 10 Gb/s equalizer off; d) 10 Gb/s equalizer on.

OOK modulation was tested up to 25Gb/s. The performed measurements are displayed in Figures 19 and 20; as can be seen, without equalization, the eye diagrams above 5 Gb/s show an intersymbol interference (ISI) increasing with the bit rate, actually at 25 Gb/s only with equalization it was possible to obtain an eye diagram.

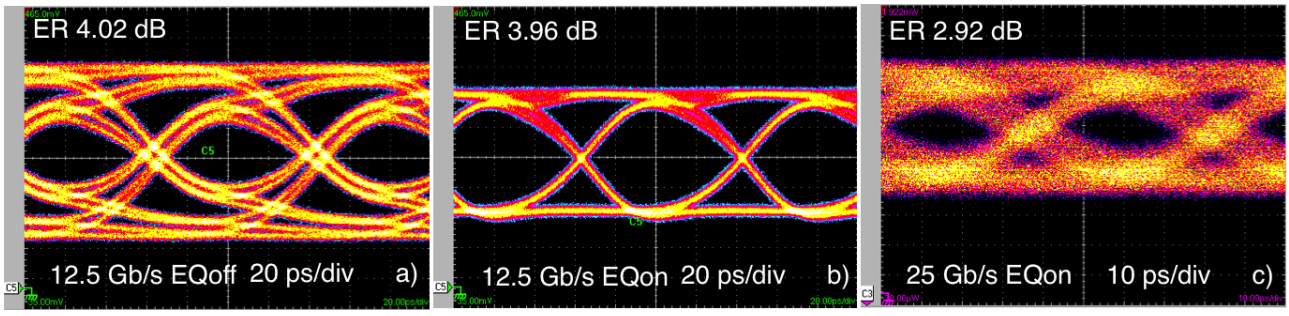

Figure 20. OOK eye diagrams: a)12.5 Gb/s equalizer off; b) 12.5 Gb/s equalizer on; c) 25 Gb/s equalizer on.

5.1.5 4-PAM modulation

As 4-PAM modulation is concerned it was possible to obtain clear eye openings at 10 Gbaud/s and 12.5 Gbaud/s only with the aid of the integrated equalizer, as shown in Figure 21.

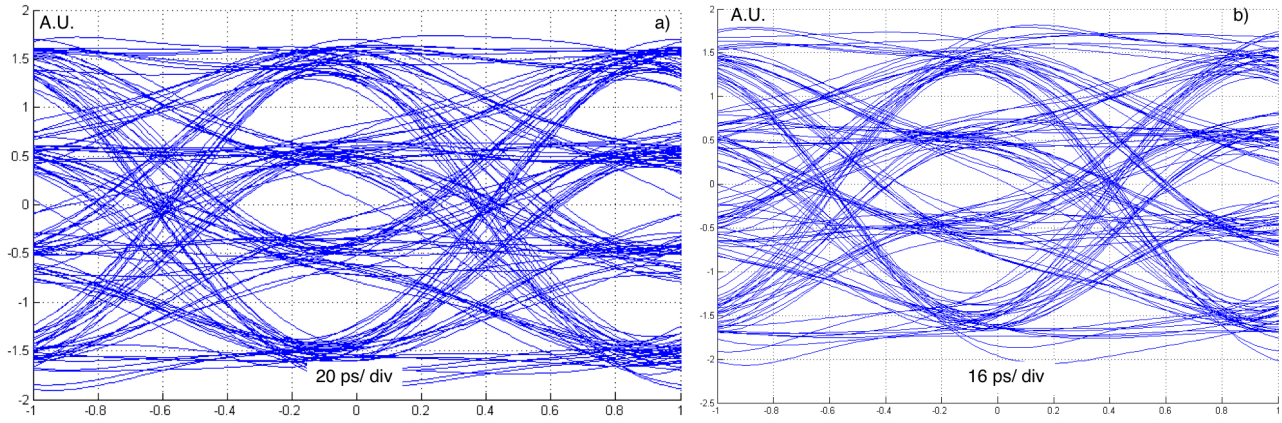

Figure 21. 4-PAM eye diagrams: a)10 Gbaud/s equalizer on; b) 12.5 Gbaud/s equalizer on.

5.2 IDT HXT44100 DRIVER TESTS

The experimental tests were performed also with the second selected driver IDT HTX44100. The operation of this driver is more critical due to the fact that it is designed for use with DFB lasers, thus with VCSELs a lower control resolution can be obtained due to the need of very low currents with respect to DFBs. Moreover the equivalent resistance is matched with 8 kΩ (nominal values) contrary to the IDT HTX14100, almost matched to VCSEL with 60 kΩ resistance. As can be seen in Figure 22 (showing the VCSEL output power electrical spectrum without RF driving signal) these conditions reflect also on the presence of frequency resonances also in absence of RF modulation.

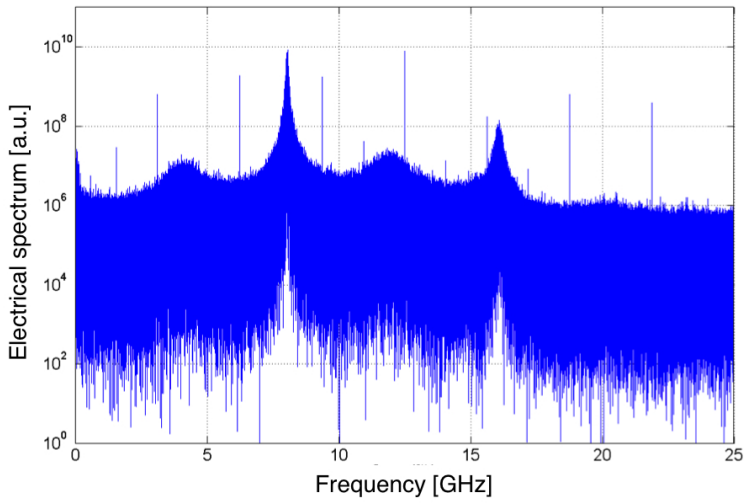

Figure 22. VCSEL output power electrical spectrum without RF driving signal.

5.2.1 CW characterization

The measured power versus current curve is shown in Figure 23 and accordingly the GUI parameters were set to obtain a bias current around 13 mA and a maximum modulation current of 10 mA: BA=15, BM=6, DTERM=2; VGAC=96.

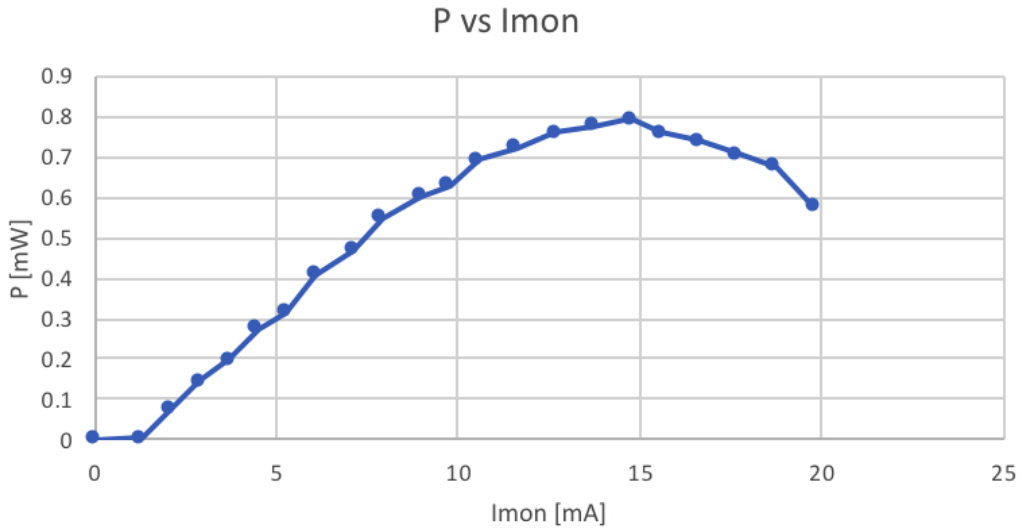

Figure 23. VCSEL output power as a function of the bias current.

Figure.24 presents the VCSEL spectra in CW mode with I_{bias} of 13 mA and under DMT modulation.

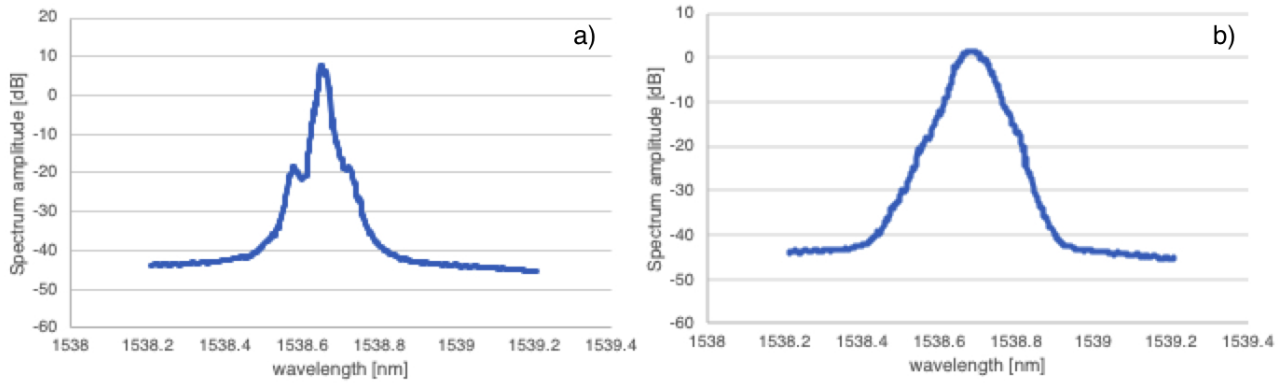

Figure 24. VCSEL optical spectrum: a) CW mode with Ibias=13mA; b) under DMT modulation with 11 mA peak-to-peak modulation depth.

5.2.2 DMT modulation for transport capacity performance evaluation

As in paragraph 5.1.3 we employed a DSB DMT modulation covering a 10 GHz bandwidth. Obtained results are presented in Figure 25. The overall supported capacity is 34.7 Gb/s also in presence of equalization; probably due to the before mentioned resonances the equalizer is not very effective. It is evident in fact that last subcarriers can support lower modulation formats if compared with Figure 17.

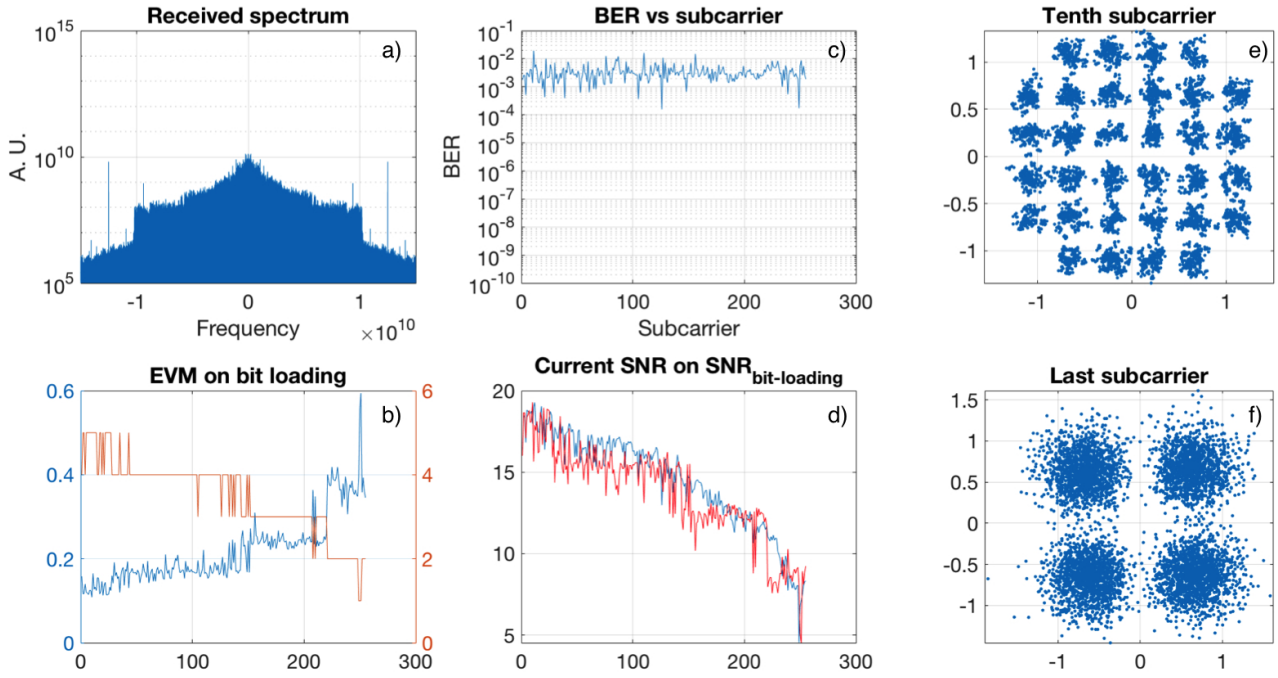

Figure 25. DSB DMT transmission over 10-GHz electrical spectrum, driver equalizer off: a) electrical spectrum vs frequency; b) EVM (blue) and bit loading (red) vs subcarrier number; c) BER vs subcarrier number; d) actual (blue) and bit-loading equivalent (red) SNR vs subcarrier number; e) tenth subcarrier constellation diagram; f) last subcarrier constellation diagram.

5.2.3 OOK modulation

Also OOK modulation showed poorer performance as can be seen from Figure 26 due to distortions and bandwidth limitations; the 10-Gb/s eye diagram shows a substantial eye closure also in presence of equalization.

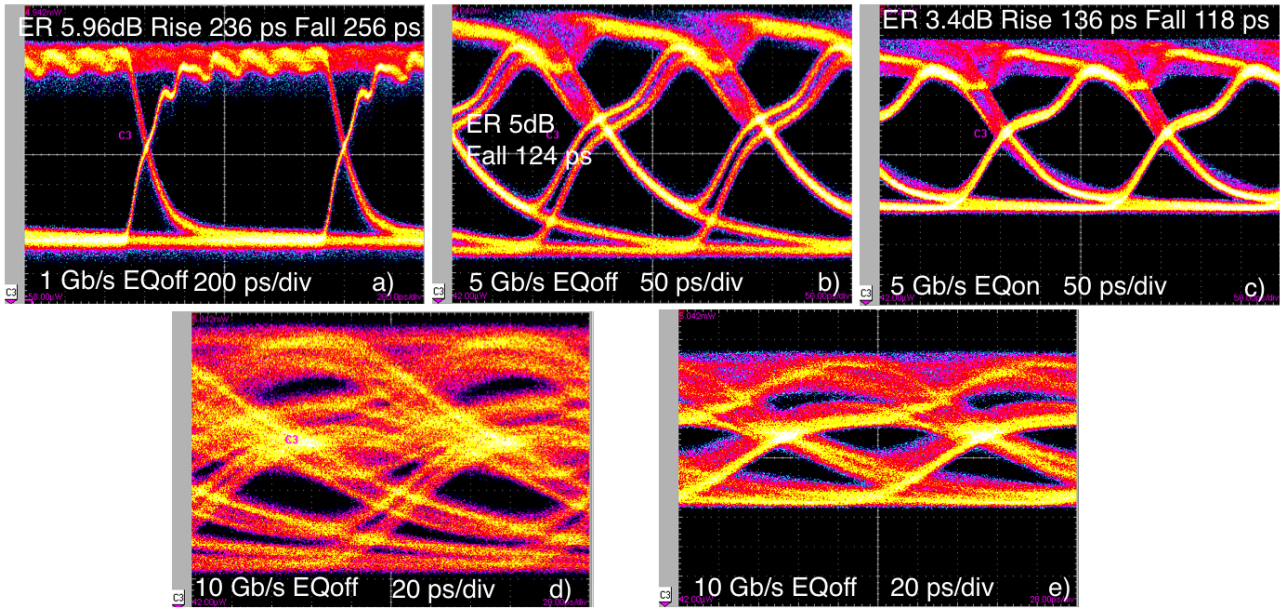

Figure 26. OOK eye diagrams: a)1 Gb/s equalizer off; b) 5 Gb/s equalizer off; c) 5 Gb/s equalizer on; d) 10 Gb/s equalizer off; e)10 Gb/s equalizer on.

5.3 MEASUREMENTS DISCUSSION

First and preliminary tests on directly modulated VCSELs exploiting selected drivers indicate that the IDT HTX14100 presents better performance both in terms of transmitted capacity and in terms of energy consumption. Moreover, the IDT HTX14100, being designed for typical VCSEL currents, is operated over its full control range and thus allows a finer command of the bias current and of the modulation depth, which is needed in the PASSION modular approach to fine tune the VCSELs in the 100-GHz range. Further tests are envisaged to evaluate the impact of bonding and of possible resistance mismatches both on the frequency transfer function and on driver operation.

6 CONCLUSIONS

In this deliverable, we have tested a selection of drivers required to control the VERTILAS VCSEL sources employed in the realization of the PASSION Tx module. In particular, the preliminary tests have been finalized to the characterization of the drivers to operate with multi-level and/or multi-subcarrier modulation formats, such as PAM and DMT. The drivers have been selected among several commercial products available on the market thanks to the required modulation bandwidth and bias current level. Also, the dimensions have been important parameters in the selection to assure a very high compact integration of multiple VCSEL-based Tx according to the modular approach described in the paragraph 2.2 and to the layout in the paragraph 2.3.
From the experimental characterizations realized in the POLIMI laboratory, the HTX14100 driver produced by IDT has demonstrated to guarantee the specifications required for the implementation of the PASSION Tx. This model is a single channel, low power, linear VCSEL driver supporting signalling rates up to 28GBuad or 56Gbps 4-PAM. It has experimentally shown its capabilities to directly drive the VCSEL with multilevel and/or multicarrier formats with a significant linear response. Moreover, the ADC bit number allows a fine control of the bias current to achieve the required wavelength emission tuning of the VCSEL. With respect to the other selected and checked driver (IDT HTX44100) a better resistance matching is guaranteed, in combination with lower power consumption.
Further experimental analysis of the impact of the bonding between the VCSEL and the driver will be performed to better understand the possible limitation on the modulation bandwidth.
According to the reported discussed experimental results, the IDT HTX14100 driver is selected as the driver for the PASSION integrated multi-channel Tx implementation.

The results presented in this Deliverable D3.2 constitute the achievement of the Milestone M3.2 “Direct modulation of VCSELs demonstrated with selected drivers”.

7 REFERENCES

[1] A. Gatto, D. Argenio, P. Boffi, “Very high-capacity short-reach VCSEL systems exploiting multicarrier intensity modulation and direct detection,” Opt. Expr., 24, 12, 12769-12775 (2016).

[2] F. Li, et al., "Optimization of training sequence for DFT-spread DMT signal in optical access network with direct detection utilizing DML," Opt. Express 22, 22962-22967 (2014)

[3] P. S. Chow et al., "A practical discrete multitone transceiver loading algorithm for data transmission over spectrally shaped channels," IEEE Trans. on comm., Vol. **43**, pp. 773-775, (1995).

[4] A. Gatto, P. Parolari, C. Neumeyr, and P. Boffi, "Beyond 25 Gb/s Directly-Modulated Widely Tunable VCSEL for Next Generation Access Network," in OFC Conference, 2018, paper Th1E.2.

8 ACRONYMS

4-PAM 4-level pulse amplitude modulation
ADC analog to digital converter
APC automatic power control
AWG arbitrary waveform generator
BTJ buried tunnel junction
CP cyclic prefix
CTLE continuous time linear equalization
DBR distributed Bragg reflector
DML directly modulated laser
DMT discrete multitone
DSB dual sideband
DSO digital sampling oscilloscope
EML electro-absorption modulated laser
FEC forward error correction
FFT fast Fourier transform
FWHM full width half maximum
GUI graphic unit interface
ISI intersymbol interference
LGA Land Grid Array
LOS loss of signal
MCF multicore fibre
MUX multiplexer
OOK on-off keying
OTP one-time programmable
PAPR peak to average power ratio
PD photo diode
PIC Photonics Integrated Chip
PMF polarization-maintaining fibre
QAM quadrature amplitude modulation
QPSK quadrature phase shift keying
RDL redistribution layers
RF radio frequency
S-BVT sliceable bandwidth/ bit rate variable transceiver
SMSR side mode suppression ratio
SNR signal to noise ratio
SOI Silicon-Over-Insulator
SSB single sideband
TOSA transmitter optical sub-assembly
TX transmitter

VCSEL vertical cavity surface emitting laser
WDM wavelength division multiplexing
WB wire bond