



DESIGN OF THE TX MODULE ARCHITECTURE AND INTERFACES

Module design, assembly strategy and opto-electrical interfaces.

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1 D3.1 PUBLIC SUMMARY - DESIGN OF THE TX MODULE ARCHITECTURE AND INTERFACES

The deliverable D3.1 contains a detailed conceptual design proposal of the transmitter (Tx) module architecture, constituted by vertically emitting laser sources (VCSEL) and able to target a capacity up to 2 Tb/s, representing a key building block for the PASSION project. As described in Fig. 1, 40 VCSELs modulated up to 50 Gb/s by exploiting DMT or PAM4 formats are hybridly mounted on a wavelength multiplexer Silicon-Over-Insulator (SOI) Photonics Integrated Chip (PIC) hereinafter Si-PIC. This module is called in the report as MOD1.

A total transmitted capacity up to 8 Tb/s is provided thanks to the aggregation of four identical modules MOD1, operating on the same optical state-of-polarization (SoP), but tuned by 25-GHz each other to cover the entire C-band. In the report, these super modules are called MODX and MODY, dependently by the specific operating SoP of the module. The module MOD1 represents the smallest discrete granularity element in the PASSION data-capacity aggregation scheme.

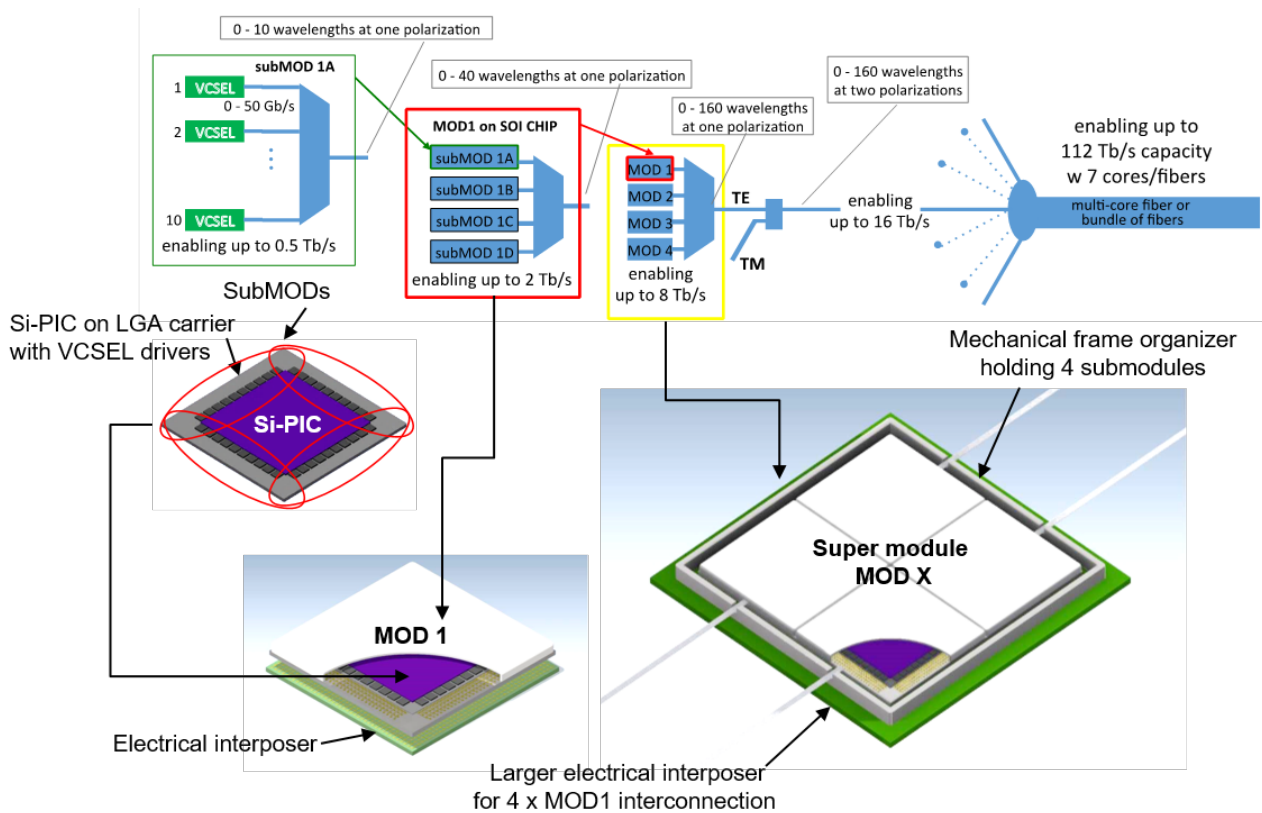


Figure 1. Structure of Tx Module MOD 1 (up to 2-Tb/s in capacity) and of a super module (MODX)

In MOD1 the 40 VCSELs are bonded and optically coupled with integrated up-reflecting mirrors on a Si-PIC. This subassembly requires constant temperature operation to prevent thermally-induced wavelength drifts. Active cooling is therefore provided to Si-PIC with a thermoelectric cooler (TEC).

Suitable long-wavelength VCSELs (wavelength range: 1530nm to 1562nm) will be designed by VERT to work at $40^{\circ}\text{C} \pm 0.1^{\circ}\text{C}$ as a reasonable trade-off to still obtain a sufficient optical output

power, minimizing TEC power consumption when MOD 1 is operating in ambient temperature ranging from -5°C to $+70^{\circ}\text{C}$.

A very short resonator length and an active region optimized for a high bandwidth will be necessary for the employed PASSION laser sources: hence, the so-called short cavity (SC) VCSEL concept will be adopted in the VCSEL design. A cross section of this design is shown in Fig. 2.

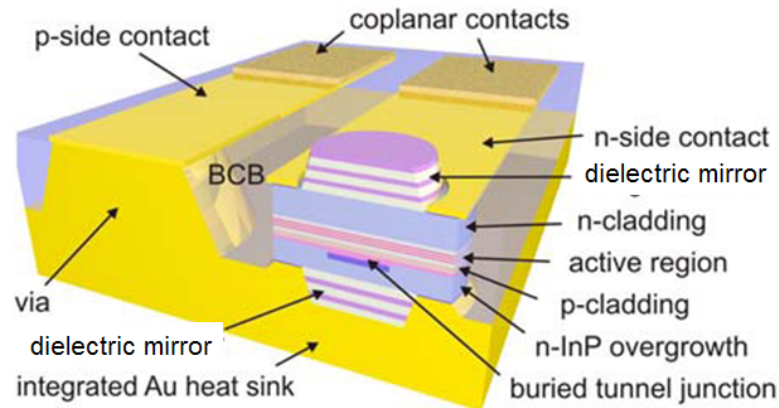


Figure 2. Cross section short-cavity VCSEL

VCSEL drivers (for thermal reasons) are expected to be outside the Si-PIC chip, but still at very short reach allowing wire bonds (WBs) to provide the necessary interconnections. However, for high-speed and high bandwidth operations WBs should be as short as possible. VCSELs will be positioned as close to the Si-PIC chip edge as possible. An optimal solution would be to place the 40 VCSELs (which correspond to the 40-channels requirement of the Si-PIC chip) close to the perimeter of the SiPh chip with 10 VCSELs on each edge.

The 10 channels on one edge of the chip are multiplexed for each sub-MOD into a single output, thanks to wavelength multiplexers (MUX), while the 4 sub-MOD outputs are combined again into another single output completing the multiplexing function within the Si-PIC chip. The two MUX stages display 400-GHz and 100-GHz spacing respectively.

The final frequency spacing between the Tx channels is 25 GHz, covering thanks to 160 channels about 4000 GHz in the C-Band. Nevertheless, there is flexibility in terms of how these channels are distributed between MODs, and within each MOD. Interleaving the channels among various MODs and sub-MODs helps in taking advantage of this flexibility in order to relax the requirements on the transmitter mux design, make them more tolerant to variations, and if possible, design mux building blocks working for multiple MODs and sub-MODs.

Different designs for the sub-MOD and MOD MUXs are proposed, based on the exploitation of arrayed waveguide gratings, Echelle gratings, and Mach-Zehnder interferometers, considering the insertion loss, crosstalk, channel non-uniformity, footprint, flexibility of the chip architecture within/between MODs.



The designed devices will be fabricated in order to test their viability. Depending on the device elements, the designs will be either submitted to the upcoming multi-project wafer run for the VTT 3 μm SOI technology platform, or dedicated runs will be pursued for realization of the devices.

Up-reflecting mirrors on Si-PIC will be used to address optical beams from VCSELs into waveguides and also to deliver optical signals toward a fibre optic assembly which similarly will use a 90° optical steering mechanism, allowing the fibre to be laid parallel to the Si-PIC surface after pigtailling. This approach will consistently improve the overall MOD 1 form-factor design.

Linear drivers will be thermally decoupled from Si-PIC in order to avoid operating at constant temperature. Their dissipated power will not be handled by a TEC, but sunk-out in air at ambient temperature with an external passive heatsink, dramatically reducing the overall MOD1 electrical power consumption.

Regarding the packaging, the proposed package design for the MOD1 will be based on a hermetic multilayers Land Grid Array (cavity package typology) holding 2200 pads. In this kind of package a specific RF redistribution layer (RDL) shielded from other RDLs (for digital controls and power supply) will be needed.



2 ACRONYMS

AWG	Arrayed Waveguide Grating
CPW	Coplanar Waveguide
DML	Directly-Modulated Laser
DMT	Dicerete Multitone Transmission
DM-VCSEL	Directly-Modulated VCSEL
EG	Echelle Grating
FSR	Free Spectral Range
FWHM	Full Width Half Maximum
I ² C	Inter-Integrated Circuit
LGA	Land Grid Array
MMI	Multi-Mode Interferometer
MOD	Basis Module (from 1 to 4)
MOD X	Super Module for TE Polarization
MOD Y	Super Module for TM Polarization
MPW	Multi-Project Wafer
MZI	Mach-Zehnder Interferometer
MUX	Optical Multiplexer
PAM	Pulse Amplitude Modulation
PD	Photodetector
PIC	Photonics Integrated Chip
PMF	Polarization Maintaining Fiber
RDL	Redistribution Layer
RF	Radio Frequency
RT	Room Temperature
SC-VCSEL	Short Cavity VCSEL
SiPh	Silicon Photonics
Si-PIC	Silicon-Over-Insulator Photonics Integrated Chip
SMSR	Single Mode Suppression Ratio
SOI	Silicon-Over-Insulator
SoP	State-of-Polarization
SPI	Serial Peripheral Interface
sub-MOD	Submodule containing 10 wavelengths
TE	Transverse Electric
TM	Transverse Magnetic
Tx	Transmitter
VCSEL	Vertical Cavity Surface Emitting Laser
WB	Wire Bond