D 1.8 PUBLIC PROGRESS REPORT 2

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EXECUTIVE SUMMARY

The deliverable D1.8 is PASSION second Public progress report.

It includes the publishable summary evidencing the overall objectives of the project, with attention to the work performed and to results achieved so far. The progress beyond the state of the art, and the expected results and potential impacts, including the socio-economic impact and the wider societal implications, are also described.

The list of achieved deliverables and milestones is reported together with the description of the main achievements obtained in the WPs in the period M13 – M24.

1 SUMMARY FOR PUBLICATION

1.1 SUMMARY OF THE CONTEXT AND OVERALL OBJECTIVES OF THE PROJECT

In the last decade we assisted to a continuous growth of the metro network, but we are now facing a bottleneck in the transmission and routing of the huge amount of data due to the dramatic increase of the number of users, the content size, and to the convergence with mobile and datacom networks. Photonics is a key enabling technology for the evolution of the entire telecommunications infrastructure, supporting increasing bandwidth requirements and quality of service (QoS), but the traditional optical technologies exploited today mainly for long haul transmission are too expensive and power hungry for the future metro network.

The aim of PASSION project is to develop new photonic technologies and devices for supporting sustainable metro networks, capable of enabling target capacities of Tb/s per spatial channel, 100 Tb/s per link and Pb/s per node over a few hundred-kms distances. A new metro network infrastructure is envisioned within the project, fitting the network operator requirements and roadmaps and offering multiple relevant characteristics that include: (i) reduced network cost, energy/power consumption and equipment footprint, that are achieved by the development of compact/cost-effective switching technologies and transmitter (using direct modulated vertical-cavity surface-emitting lasers, VCSELs) and multi-channel coherent receiver modules with dense photonic integration; (ii) increased system flexibility and modularity by the adoption of sliceable bandwidth/bitrate variable transceivers (S-BVTs) with reconfigurable parameters; (iii) increased network and system scalability, programmability and reconfigurability, that are enabled by agile aggregation in the spectrum, polarization and space dimensions and the implementation of a software defined networking (SDN) control platform.

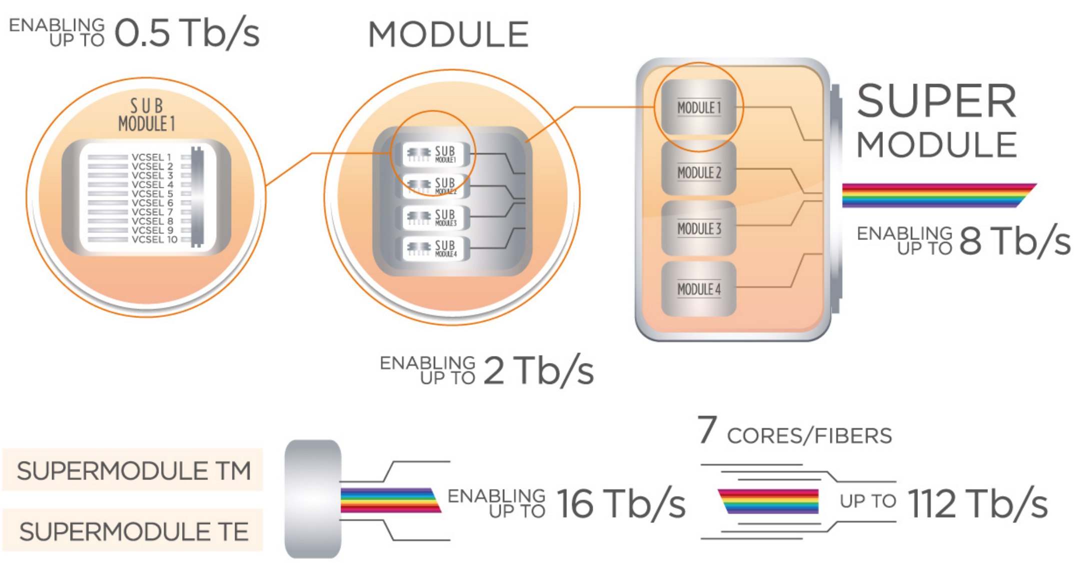

Figure 1. PASSION S-BVT Tx based on the modular approach.

In particular, Figure 1 shows the S-BVT Tx based on the modular approach: the module integrating 40 VCSELs in Silicon photonics capable of enabling up to 2 Tb/s aggregated capacity constitutes the building block of the S-BVT. By combining four of such a module, a full 160-channel Tx supermodule is obtained with 25-GHz granularity over the whole C band and with up to 8 Tb/s capacity. By exploiting also polarization-division multiplexing and spatial multiplexing, coupling two supermodules outputs orthogonal in polarization and exploiting bundles of fibers or multi-core fibers, PASSION Tx is able to reach a capacity per link higher than 100 Tb/s.

PASSION network platform is also realized by means an innovative energy-efficient and small-footprint node approach, adopting different technologies: flex-grid aggregation/disaggregation/add switches; high-connectivity multicast switches, and large-port photonic polymer PLC-based space switch matrixes. Such a S-BVT based network architecture (Fig. 2) with 25-GHz fine granularity guarantees reconfigurability and flexibility at different levels (in spectrum, polarization and space), and scalability to support a “pay-as-you-grow” scheme. SDN ensures network programmability, fitting network operator requirements and roadmaps.

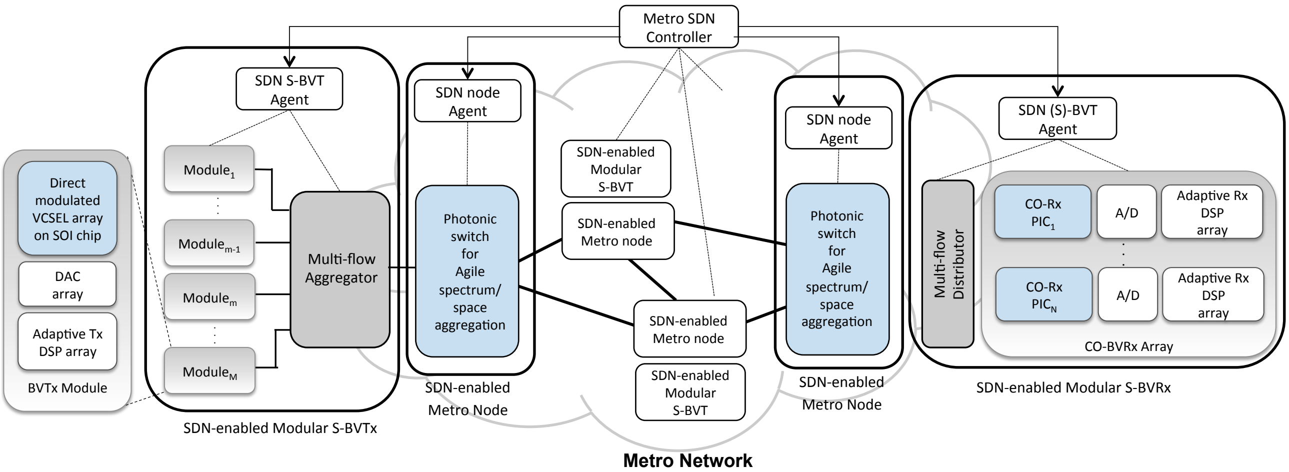

Figure 2. PASSION metro network envisioned infrastructure.

1.2 Work performed from the beginning of the project to the end of the period covered by the report and main results achieved so far

After 24 months from the start of the project (December 1st, 2017) 22 PASSION deliverables have been completed (3 in delay) and 12 milestones have been achieved (1 in delay). In particular, in addiction to outcomes related to the project management and dissemination (such as the PASSION website, the dissemination and data management plans), we achieved important scientific results reported in the following.

- Definition of use cases and requirements for the PASSION network, systems and sub-systems. Considering the targeted uses cases, a detailed definition of the metro network architecture divided into a number of hierarchical levels supporting different aggregated data traffic volumes and operating at heterogonous granularities has been provided. Moreover, the node and the transceiver architecture have been defined.

- Definition of the technological circuitry matching the functionalities required by the PASSION optical node. Photonic integrated circuits able to handle the add/drop traffic and traffic aggregation/disaggregation functionalities with a modular approach have been identified and designed with the aim to deliver on-chip switch node functionalities for flexible Pb/s capacity. The design of both monolithic InP and hybrid SiPh wavelength selective switches (WSSs) has been completed. The fabrication is ongoing. The design, fabrication and testing of a folded WSS has been completed. This design the number of required arrayed waveguide gratings (AWGs) by half and hence reduces the footprint.

- Detailed design of the 40-VCSELs Tx module architecture targeting up to 2 Tb/s aggregated capacity. The SiPh architecture with multiple VCSELs bonded and coupled on a SOI-based Si-PIC embedding wavelength multiplexing capabilities has been developed. According to the chosen assembly strategy, optical and electrical interfaces have been realized. Preliminary test of the VCSEL sources supported by the selected electrical drivers has been performed. First wafer runs for the VCSELs matching the PASSION requirements have been completed. SiPh chips for the 2-Tb/s module realization have been fabricated and tested.

- Development of the process and the building blocks to enable the monolithically integrated coherent receiver submodule per each channel. Two tunable laser concepts have been selected, fabricated and characterized. Preliminary local oscillator (LO) laser linewidths show typically <150kHz over the C-band. An updated design of tunable laser to address control and calibration aspects was taped-out. Design and tape-out of a dual-polarization integrated coherent receiver (ICR) including several de-risk measures. First prototype of ICR (single polarization) has been designed and is being manufactured.

- Design of the scalable S-BVT architecture, considering the different components and identifying the S-BVT requirements, parameters and features, including the modularity, granularity and slice-ability. Key control functionalities to be handled by the SDN controller and the control interfaces have been developed.

1.3 Progress beyond the state of the art, expected results until the end of the project and potential impacts (including the socio-economic impact and the wider societal implications of the project so far)

The fulfilment of PASSION main goal is the availability of an application driven photonic technological platform for the development of a new generation of low-cost, energy-efficient and reduced-footprint devices, modules and sub-systems exploiting the synergy between directly-modulated VCSEL capabilities with massive integration in Silicon Photonics, multichannel coherent detection, innovative switching technologies and spectrum/space aggregation. They will support a radically new sustainable modular and scalable network architecture for the metro segment. In this perspective, PASSION is expected to significantly impact on the metro network architecture, based on the superimposition of the spectrum and space aggregation. Scalability arises as a key functionality to be considered in the design of the envisioned metro network architecture in order to easily expand/upgrade the network according to the existing and future traffic demand. Hence, a programmable and modular approach becomes crucial to enhance network scalability without requiring significant re-engineering of the existing infrastructure.

The innovation potential of the European photonic companies and notably of the SMEs involved in the project will be improved by the cooperation along the value chain in PASSION. PASSION is a multi-disciplinary project requiring optical design, integration design, packaging design, system design as well as network design skills. Each Partner will focus on his core competences in terms of his resources and infrastructures, while relying on other Partners, thanks to already-established long-lasting relationships, with a new open access infrastructures and services to design, prototyping manufacturing and testing.

2 Deliverables (M13 – M24)

Del. No.	Deliverable name	WP No.	Lead benef	Type	Diss level	Deliv date	Submis date	Comments
D4.2	First generation of hardware efficient modular coherent receivers	WP4	EFP	R	CO	M12	22/02/19	Document produced within WP4 “Switching, aggregation and Rx photonic technologies” describing the measurement results of the first generation of PASSION receiver chips. The deliverable has been submitted with a delay due to unexpected delays in the foundry, out of PASSION control.
D3.3	Detailed design of the SiPh PICs and the Tx submodules	WP3	VTT	R	CO	M13	09/01/19	Document produced within WP3 “Photonic technologies for Tx” defining the detailed design of the SiPh PICs and the Tx submodules.
D5.1	Final test-bed design and development plan	WP5	SMO	R	PU	M18	31/05/19	Document produced within WP5 “Integration and demonstration of photonic devices and technologies” providing a description of the implementation, integration and demonstration plans to be performed during the project.
D3.4	Test results from passive SiPh PICs integrated with VCSELs	WP3	TUE	R	PU	M15	14/06/19	The document is the deliverable D3.4 of PASSION Project. It is a document produced within the Work Package 3 “Photonic technologies for Tx” and it provides a description of the design, fabrication and testing of the co-integration of VCSELs with passive SiPh PCIs. The deliverable has been submitted with a delay due to lack of accessibility to machines and processes.

D3.5	Intermediate report on the development of directly modulated VCSELs	WP3	VERT	R	PU	M18	20/06/19	The document is the deliverable D3.5 of PASSION Project. It is a document produced within the Work Package 3 "Photonic technologies for Tx" and it describes the development of the new VCSELs matching the PASSION requirements. The deliverable has been submitted with a delay due to some issues in the first new wafer runs.
D4.3	Low power consumption and agile wavelength selecting switches	WP4	TUE	R	PU	M17	24/06/19	Document produced within WP4 "Switching, aggregation and Rx photonic technologies". Owing to a delay in the arrival of the fiber array with suitable pitch and in VTT process to produce their own fiber array, the deliverable has been submitted with a delay.
D4.4	SiPh circuitry for hybrid integrated low insertion loss MCS	WP4	TUE	R	PU	M20	31/7/19	Document produced within WP4 "Switching, aggregation and Rx photonic technologies". It provides a description of the design of SiPh circuitry for hybrid integrated low insertion loss multicasting switches including spectrum slicing and space switching.
D4.5	Process development and fab run of PI WDM SOAs	WP4	TUE	R	PU	M22	in delay	Document produced within WP4 "Switching, aggregation and Rx photonic technologies". Owing to a delay in the delivery of polarization independent SOAs and in TUE chip characterization, the deliverable is expected to be submitted in the first week of M25.
D4.6	Second generation of hardware efficient modular coherent receivers	WP4	EFP	R	CO	M22	in delay	Document produced within WP4 "Switching, aggregation and Rx photonic technologies". Owing to some supply chain issues (e.g. in TIA and PCB/PCBA supplier), the

								deliverable will be submitted at the beginning of 2020.
D3.6	Test results from the first transmitter submodule with directly modulated VCSELs	WP3	VTT	R	PU	M23	in delay	Document produced within the WP3 "Photonic technologies for Tx". Owing to the need of a new re-tape and manufacturing-run of the electrical interposer for the TX module due to wrong information about the pad coordinates of the selected VCSEL drivers released by the supplier.The deliverable will be submitted in delay, at the beginning of 2020.
D1.7	Second periodic report	WP1	POLIMI	R	CO	M24	29/11/19	Document produced within WP1 "Project management and coordination" related to the second report (M13-M24), about the full financial, technical and risk management progress.
D1.8	Public progress report 2	WP1	POLIMI	R	PU	M24	29/11/19	Document produced within WP1 "Project management and coordination" related to the second public progress report (M13-M24).
D6.3	Report on industrial-oriented and scientific oriented dissemination activities 2	WP6	VLC	R	PU	M24	30/11/19	Document produced within WP6 "Exploitation plan, dissemination and standardization" related to the second report (M13-M24) about the scientific oriented dissemination activities.

3 Milestones (M13 – M24)

Milestone	Milestone name	WP no	Lead benef	Delivery date	Subm date	Mean of verification	Achieved
MS5	Design completed for SiPh PICs and Tx submodules	WP3	VTT	01/01/19	01/01/19	Deliverable D3.3 "Detailed design of the SiPh PICs and the Tx submodules" upoladed on January 9th, 2019.	YES
MS6	Preliminary definition of the node and transceiver architecture	WP2	CTTC	01/02/19	31/01/19	Document PASSION_WP2_MS6_v0 .2.pdf uploaded in the PASSION repository on January 31th, 2019.	YES
MS7	Efficient coupling	WP3	TUE	01/03/19	14/06/19	Deliverable D3.4 "Test results from passive SiPh PICs integrated with	YES

	demonstrated between VCSELs, SiPh PICs and fibers					VCSELs" uploaded on June 14th, 2019.	
MS8	Definition of improved design for second generation of multichannel coherent receivers on InP	WP4	EFP	01/03/19	15/03/19	Document PASSION_WP4_MS8_v1.0.pdf uploaded in the PASSION repository on March 20th, 2019.	YES
MS9	Definition of the demonstration test-bed and hardware integration	WP5	SMO	01/04/19	01/04/19	Document PASSION_WP5_MS9_v1.0.pdf uploaded in the PASSION repository on April 18th, 2019.	YES
MS10	Low power consumption and agile wavelength selecting switches on InP	WP4	TUE	01/05/19	20/06/19	Deliverable D4.3 " Low power consumption and agile wavelength selecting switches " uploaded on June 24th, 2019.	YES
MS11	Identification of key building blocks for techno-economic analyss	WP2	TID	01/06/19	14/06/19	Document PASSION_WP2_MS11_v1.0.pdf uploaded in the PASSION repository on June 14th, 2019.	YES
MS12	First on-chip integrated arrays of PI WDM SOAs	WP4	TUE	01/10/19	29/11/19	Deliverable D4.5 "Process development and fab run of PI WDM SOAs"	YES
M13	First transmitter subassembly fabricated and tested	WP3	VTT	01/11/19	in delay	Deliverable D3.6 " Test results from the first transmitter submodule with directly modulated VCSELs " to be uploaded at the beginning of 2020.	NO

4 WPs ACHIEVEMENTS (M13 – M24)

PASSION project is characterized by a very fruitful collaboration among the partners, who periodically meet in WebEx calls and in face-to-face meetings. People can find information about the project development on the PASSION website, where the project achievements and events are continuously promoted to both general public and experts' audience. Moreover, the community is updated by the social media channels, such as Twitter, LinkedIn and Facebook.

From the network point of view, after the definition of use cases, the activity has been focused on the design of the APIs to enable the automatic programmability of the PASSION adopted network element and devices. A routing and spectrum assignment (RSA) algorithm have been devised, providing on-line path computation seeking for feasible end-to-end routes whilst attaining an efficient use of network resources.

A first definition of the node and transceiver architecture has been achieved. Considering the technologies and devices developed in WP3 and WP4, a modular and scalable S-BVT architecture, based on VCSEL-based fundamental SOI-chip modules and coherent receiver modules, has been defined targeting multi-Tb/s capacity (aggregation of multiple data flows at 50 Gb/s). This is achieved by suitably exploiting both the spectral (at sub- and super-wavelength granularity) and spatial dimensions, envisioning the adoption of direct multicarrier modulation (with bit and power loading) of the multiple VCSELs (operating in the C-band at 25-GHz spaced wavelengths for the fully-featured S-BVT) and the use of multiple fibers in a bundle or multiple cores in a multi-core fiber (MCF). Considering the different aggregation levels and the technologies developed in WP4, a simplified and more cost-effective design has been defined for HL4 nodes; while, for HL3 and HL2/HL1 nodes, more components and advanced functionalities, able to exploit both the spectral and spatial dimensions, are included. Feasibility studies have been conducted to assess the proposed approach, taking in account the filtering stages, the target capacity per flow and the adopted technologies. A techno-economic analysis of the PASSION solutions is on-going. In fact, S-BVTs are key devices to reduce IT resources and transceivers, thanks to their capability to adapt to the actual traffic demand and to obtain multiplexing gains at the optical level.

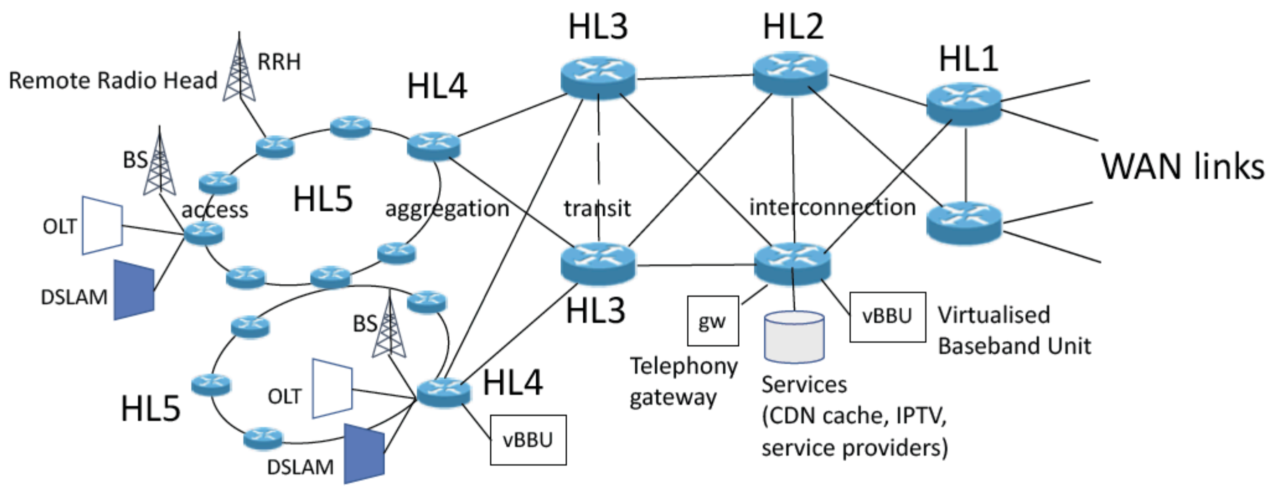

Figure 3. Schematic IP layer view of the hierarchy of routers.

Regarding the development of the photonic technologies for the transmitter, several wafer runs have been completed for the realization of the short-cavity PASSION VCSELs covering 40 ITU channels from 1530 nm to 1562 nm, optimizing the epitaxy growth for both 2" and 3" wafer equipment. The co-integration of VCSELs and SiPh photonic integrated circuit (PIC) leverages on total internal reflection mirrors (TIR) based on the VTT 3µm SOI waveguides platform. The VCSELS are flip-chip (F/C) bonded directly on top of the wafer surface, largely enabling wafer-level packaging (WLP) approach for volume manufacturing. Up-reflective and down-reflective mirrors have been embedded within SOI wafers to steer and couple VCSEL beams into respective SOI waveguides.

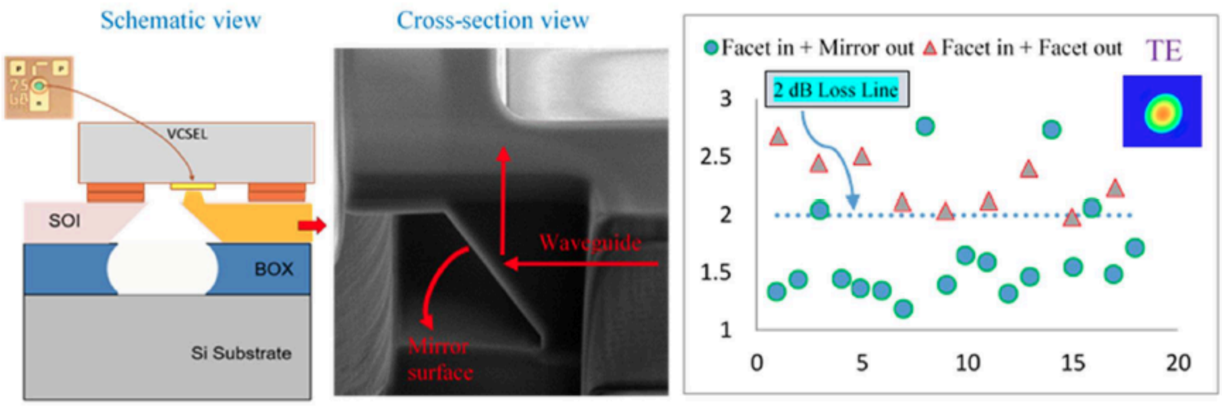

Figure 4. Schematic illustration of VCSEL integration on top of 3 µm SOI chip with up-reflecting TIR mirror in the SOI layer (left). Image of the TIR mirror cross-section taken with FIB+SEM (middle). Measurement results for insertion loss (in dB) of a 3 µm SOI chip between two lensed fibers (right).

Preliminary tests for the assembly and packaging of CMOS and VCSEL chips with a Si-PIC into a transmitter submodule have been performed while full E/O tests on the totality of the chips are still ongoing. An LGA interposer has been realized. Two hermetically sealed metal covers have been also sealed in position to provide adequate thermal contacts for Si-PIC and linear drivers respectively. A thermoelectric cooler (TEC) will be used as a constant temperature pool system. A standard passive heatsink will be used to sink-out the power generated by VCSEL drivers bonded on the LGA interposer. A mechanical clamping system has been also designed and implemented to assure high precision MOD1 positioning and contact when placed on external boards. An evaluation board (EVB) has been designed to host the 40-VCSEL module in the center of the board and routs whole electrical lines 40 VCSEL drivers and control-interfaces. A printed circuit board (PCB) has been consequently realized. The assembly of electronic components and RF connectors on the EVB is currently in progress.

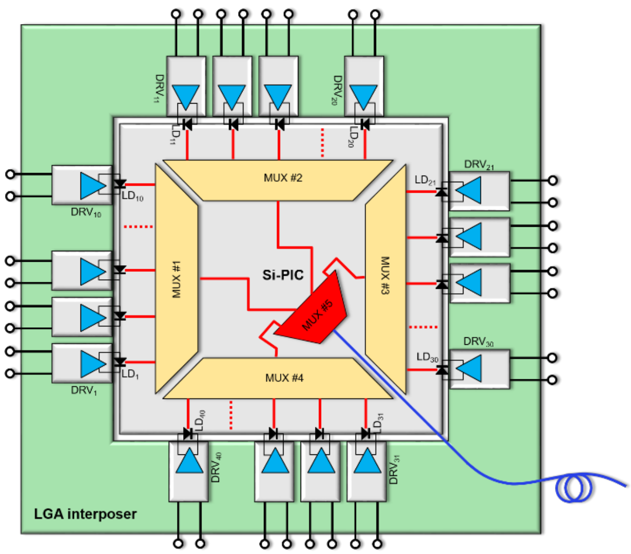

Figure 5. 40-VCSEL module structure.

Regarding the node development, initial activities toward the realization of flex-grid WSS has started. Test structures for polarization independent AWGs with channel spacing of 50 GHz and 100 GHz was designed and are currently being fabricated. Hybrid wavelength blocker (WBL) with 10, 100 GHz spaced channels are currently under fabrication. The sub-component of the multi-cast switch

(MCS), 8x1 space switch is designed. Hybrid MCS based on the hybrid co-integration of low-loss SiPh passive circuitry consisting of spectral slicing functionality with InP SOA are designed. The overall MCS is currently under fabrication. The 4x4 polymer switch has been fabricated and packaged. The switch driving board is revised for 16x16 matrix switch. The design and tape-out of a dual-polarization coherent receiver including de-risk measures have been performed. First prototype of single polarization coherent receiver is being manufactured together with the characterization of tunable laser design.

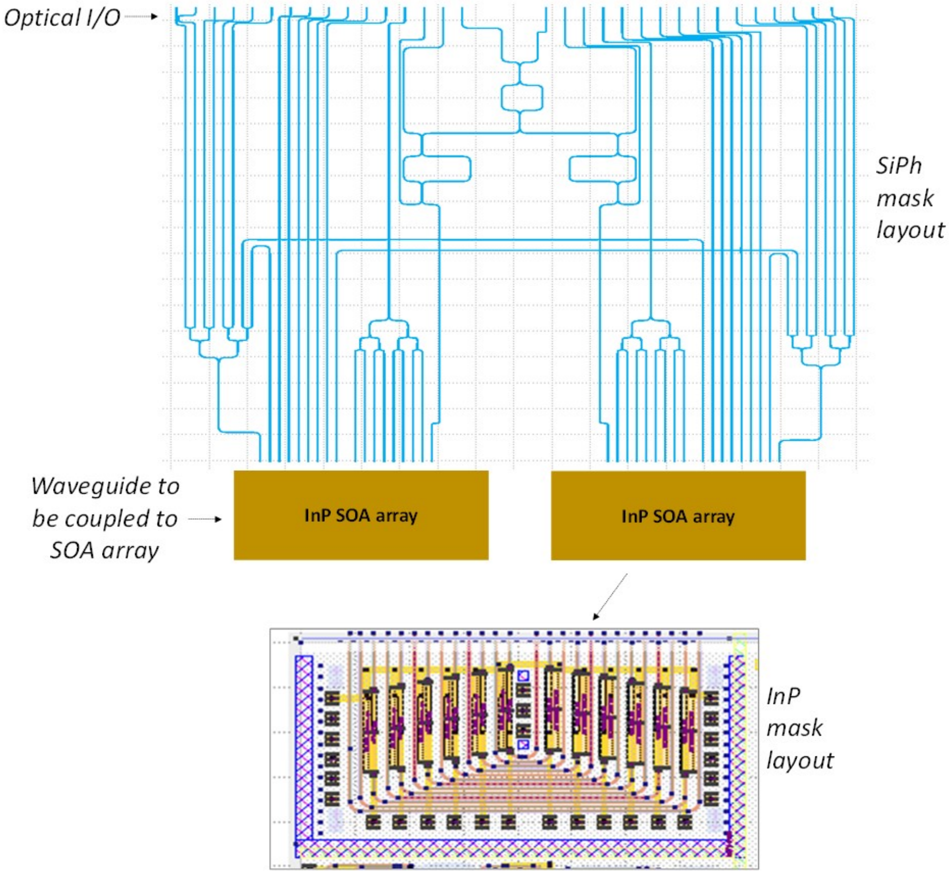

Figure 6 Mask layout of SiPh circutry and InP SOA array chips to be used for 1x2 hybrid MCS

Regarding the integration and the demonstration of the PASSION photonic devices and technologies, the activity concerning the implementation and validation of the SDN control for the network programmability as well as some of the SDN supported functions such as the actual path computation (RSA) has started. Several lab-trials have been envisioned and prepared for the verification of the final outputs per each of the other technical WPs. The integration activities have started with the development of the PCBs and/or evaluation boards for the integration of the developed components/devices.

The results achieved during this second year have been presented in 29 congresses and workshops, in 24 proceedings, journals and magazines, and have been promoted on PASSION social media channels.