D4.3 Low power consumption and agile wavelength selecting switches

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TABLE OF CONTENTS

TABLE OF FIGURES

EXECUTIVE SUMMARY

PASSION introduces new photonic technologies and devices for supporting agile metro networks, capable of enabling target capacities of Tb/s per channel, 100 Tb/s per link and Pb/s per node over increased transport distances in the range of few hundreds of kilometers. The modularity and programmability (via Software Defined Networks: SDN) of the system components of the node is used to achieve the flexibility and agility level demanded by the dynamic traffic, channel bandwidth/path/state/energy requirements of the metro network.

The PASSION switching nodes are designed to function as a reconfigurable add and drop multiplexer (ROADM) within metro core and access network. Implementation of small-footprint and low-power consumption agile wavelength selective switches (WSS) for a node featuring aggregation/disaggregation network functionalities are important criteria.

This deliverable document reports the design, and packaging activities of a low power consumption agile WSS. The agility in the WSS is achieved via dynamic selection of desired channel in the 25 GHz spectral grid. The strategy for lowering power consumption of the WSS is approached by reducing the optical loss in the switching circuit. In order to realize low power consumption agile WSS, two approaches are followed.

The first approach is a monolithic integration of the WSS, where the AWG passives and the SOA actives are all integrated in the same InP chip. The low coupling losses are enabled by designing spot-size converters. In this regard, a 1x8 WSS equipped with spot-size converters is designed and is currently under fabrication.

In the second approach, i.e. hybrid integration, the switching functionalities are realized in two target platforms in order to achieve the desired device compactness, i.e. the passive components of the WSS will be implemented in VTT's SiP technology while the SOA switching gates are implemented in InP technology. For the hybrid integration of WSS, SiP passive chip containing AWG deMux/Mux elements is designed, while at the same time an InP SOA array chip is designed and is currently under fabrication. Flip-chip bonding technique developed by VTT will be used to realize the hybrid SiP-InP WSS units in a modular units.

Scalability of the switches to high channel count/capacity is done by following a modular approach in a pay-as-you-grow manner. The InP actives are used not only to serve as switching gates but also as booster of the input signal of the WSS. The power consumption of the WSS units is significantly reduced by a low-loss hybrid integration of InP actives with SiP passives or spot size converters in case of monolithic integration. In both cases, target coupling losses of less than 2dB/facet are considered. As a result, the on-chip amplification gain is pumped only to compensate for the loss of the SiP passives. The SOA switching gates will then be driven with low gain to provide the desired extinction ratio, thereby limiting their noise contribution. By biasing the SOAs at low current values, the heat dissipation decreases. This also leads to low power consumption of the switches.

1 INTRODUCTION

1.1 BACKGROUND AND MOTIVATION

The PASSION project works towards the development of application driven photonic technologies supporting innovative transceivers and optical nodes featuring different levels of aggregation (in spectrum, and space) for an envisaged network architecture (shown in Fig.1) able to match the growing traffic demand in the metro connections. The PASSION approach is capable of establishing high capacity connection for metro network distances (typical few hundreds of km) with high throughput, low-cost, energy-efficient and reduced footprint devices for massive deployment. End-to-end connectivity for novel services and businesses is achieved with dynamic SDN control of the different systems and subsystems to ensure metro connectivity and deployment of services.

PASSION introduces new photonic technologies and devices for supporting agile metro networks, capable of enabling target capacities of Tb/s per channel, 100 Tb/s per link and Pb/s per node over increased transport distances in the range of few hundreds of kms. The modularity and programmability (via Software defined networks: SDN) system and subsystem components is used to achieve the flexibility demanded by dynamic traffic, channel bandwidth/path/state/energy requirements of the metro network.

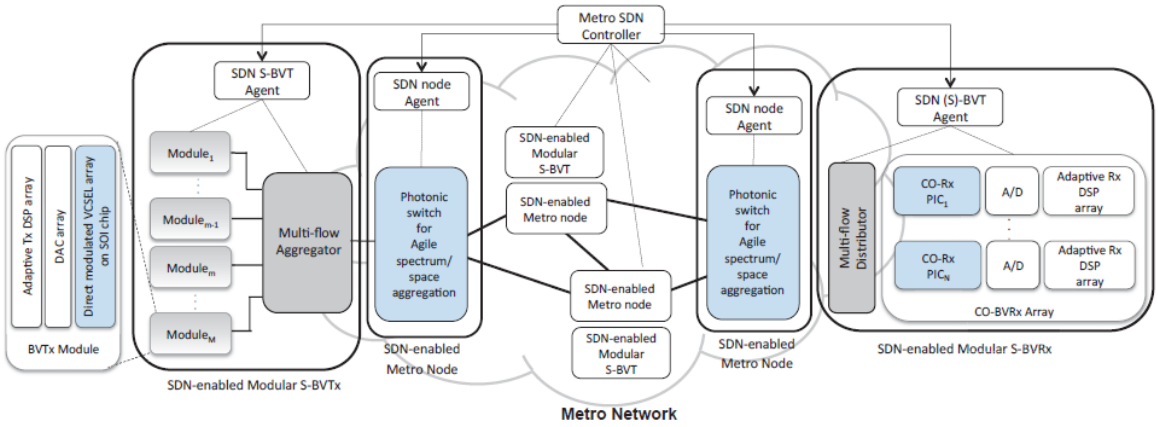


Figure 1. PASSION metro network: envisioned infrastructure, supported by new device technology developments

The growth of internet traffic and particularly bandwidth intensive application such as video, coupled with dynamic and mobile data sources are the driving wheels behind the demand for provisioning of transparent and agile metro networks [1]. To be able to effectively utilize the available spectrum and to allow compatibility with the pre-existing transmission systems, it is very essential to enable agile wavelength selective switching that allows flexibly routing different slices of the spectrum [2-3]. Reducing the power consumption of the WSS units is crucial, given the increasing energy demands of global telecommunications infrastructure [4].

Therefore, PASSION envisions the development of energy-efficient and small-footprint switching technologies for a node featuring functional aggregation/disaggregation together with switching in space and wavelength. This will in turn enable to effectively leverage the available traffic pipes in an agile manner. Compact wavelength selective switches (WSS) with low electrode number and low insertion loss will be designed.

The use of both monolithic and hybrid approaches in the switching node design will enable low fiber-to-chip coupling losses thereby lowering the energy consumption of the nodes. This deliverable report discusses the design, realization via monolithic and hybrid integration of the agile WSS, and experimental characterization of the WSS elements (deMux/Mux units and SOA gates).

1.2 TARGET OBJECTIVES

For the realization of agile WSS units, circuit design will be implemented on two different integration platforms (SiP and InP) in parallel, in order to push chip compactness and reduce power consumption. The main components for the Disag/ Aggreg/ Add data path is the agile WSSs used for filtering the channels, and switching based on wavelengths. Hence, the following strategies will be adopted for the realization and demonstration of low-power consumption, agile wavelength selective switches.

1. SiP passives (Arrayed waveguide grating (AWG) and Echelle gratings (EG)) will be used as de-Multiplexer and multiplexer units while InP SOA actives serve as switching gates. To achieve the level of agility, a dense 25 GHz grid channel spectrum design of the WSS is adopted. By turning on one or more of the consecutive 25 GHz spaced channels, agility both in bandwidth as well as central wavelength is achieved.

2. Aggressive optical loss reduction is sought through hybrid integration of passives on SiP with InP active elements. This will need careful design of SOA arrays and placement of the same to avoid material stresses and to optimize area usage for smaller footprint. Flip-chip bonding technology developed by VTT will be used to enable low-loss hybrid coupling of InP with SiP. An alternative approach to the hybrid integration is sought via monolithic integration of an InP based WSS which combines the deMux/Mux passives with the SOA actives in a single chip. The chip-to-fiber coupling loss is reduced via on-chip spot-size converters (SSCs).

3. Characterization of SiP passives and discrete SOA arrays is conducted for performance verification of elements of a low-power consumption of agile WSS. The characterized devices are on-chip SiP passives (AWG and EGs) and discrete SOAs. These tests provide a baseline for the performance verification of the hybrid integrated agile WSS structure and its scalability.

2 AGILE WAVELENGTH SELECTIVE SWITCHES (WSS)

2.1 PRINCIPLES OF OPERATION

The main approach of achieving agility in the WSS is done by enabling the switching of spectral slices in the 25 GHz grid spectrum. The PASSION spectrum has a total of 160 channels spaced by 25 GHz as illustrated in Fig. 2. Hence, the central wavelength is agile in steps of 25 GHz. The bandwidth tunablity is achieved by selecting one or more of these 25 GHz wide channels.

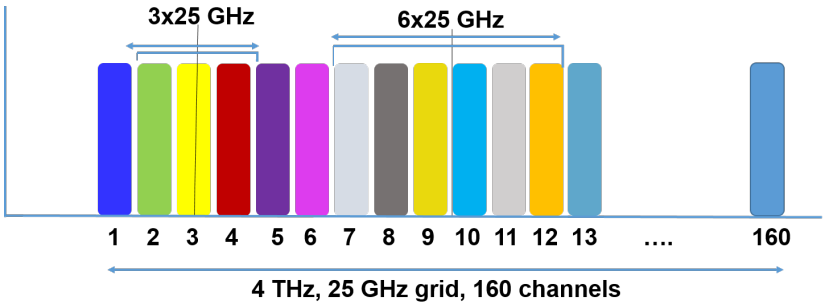


Figure 2. 25 GHz flexgrid, 4 THz spectrum,160 channels

Fig.3 shows the schematic representation of a 1x2 WSS structure based on SOA switching gates. A 1x2 WSS consists of a power splitter (PS) and two wavelength blockers (WBL). In order to realize de-multiplexing of 160 channels with 25GHz grid, the principle of modularity is employed as explained in Deliverable 4.1. A de-interleaving structure is used to transform the dense 25 GHz grid to sparser 100 GHz grid. Each output of de-interleaver is connected with a WSS consisting of 40 channels each. The four outputs of the de-interleaver are each shifted in steps of 25 GHz from each other. Within a 1x2 WSS module, a separate WBL at the channel spacing of 100 GHz is employed.

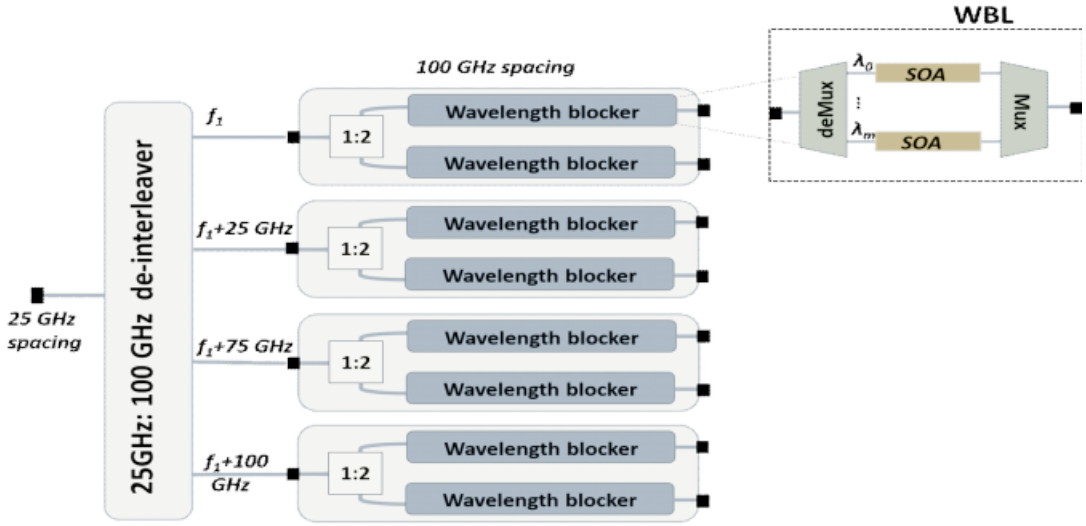


Figure 3. Representation of a 1x2 WSS, modular implementation agile WSS structure with 1:4 de-interleaver (25 : 100 GHz)

Each WBL in a module is shifted in steps of 25 GHz to match the de-interleaver outputs.

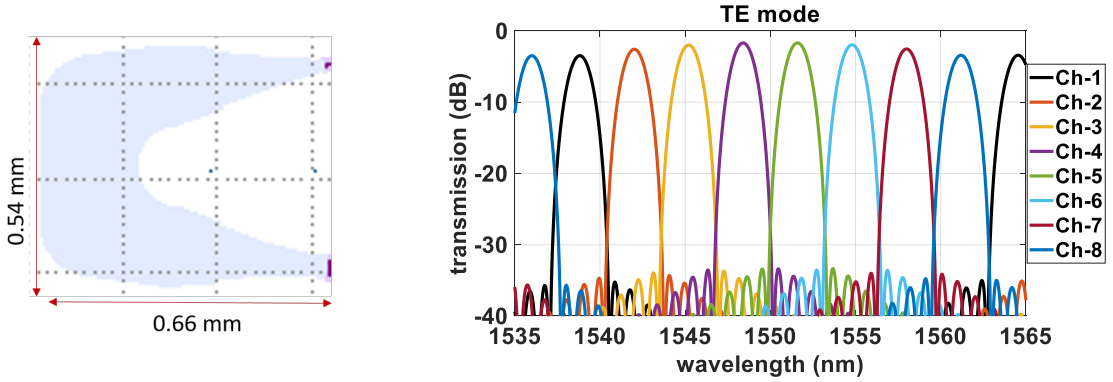
Achieving low power consumption of the WSS units is an important requirement addressed in this deliverable. This is tackled by minimizing the insertion loss of the on-chip WSS structure and avoiding power-hungry optical amplification that would be required otherwise. For this, two integration strategies of the WSS are followed. The first one makes use of monolithic integration that incorporates the de-multiplexing/multiplexing passives (AWGs) and the SOAs. In addition to switching, the SOAs provide amplification to compensate on-chip losses. Specially designed waveguides will be used to provide minimal coupling losses of the InP chip. The second strategy makes use of hybrid integration, where low-loss, polarization independent passives (AWGs) on SiP can be packaged with SOA actives (gate switches) in InP. The packaging makes use of a low-loss flip-chip bonding technology of VTT targeting coupling loss less than 2 dB/facet.

2.1 Monolithic Integration (InP WSS)

The monolithic implementation of the WSS units in InP targets the design of passive deMux/Mux units together with SOA actives in a single InP chip.

2.1.1 AWGs

A polarization independent AWG with a channel spacing of 400 GHz is designed for the realization of a monolithic integration of a 1x8 WSS in a single InP chip. This InP chip contains sixteen 400 GHz AWGs. The target channel spacing of 400 GHz is selected since it has better tolerance against process induced phase variations/errors than AWGs with lower channel spacing. The mask layout of a polarization independent 400 GHz AWG is shown in Fig. 4(a) and it occupies a footprint of 0.54 mm x 0.66 mm. Fig.4 (b) shows the transmission response for TE mode. It has insertion loss from 1.6-3.5 dB. Similar response is designed for TM-mode to enable polarization independent operation.



(a) (b)

Figure 4. (a) Masklayout of a 400 GHz, 8-channel InP AWG with polarization independent features (b) transmission response (TE mode)

2.1.2 WSS Design

The schematic representation of a monolithically integrated polarization independent 400 GHz, 1x8 WSS structure is shown in Fig. 5(a). The loss-less performance of this InP chip is enabled by a spot-size converter (SSC) structure that adapts the mode-profile of an InP chip to that of a 10-μm single mode fiber (SMF) both at the input-and outputs. The SSCs optimized length is 2000 μm for target coupling loss values less than 2dB/facet.

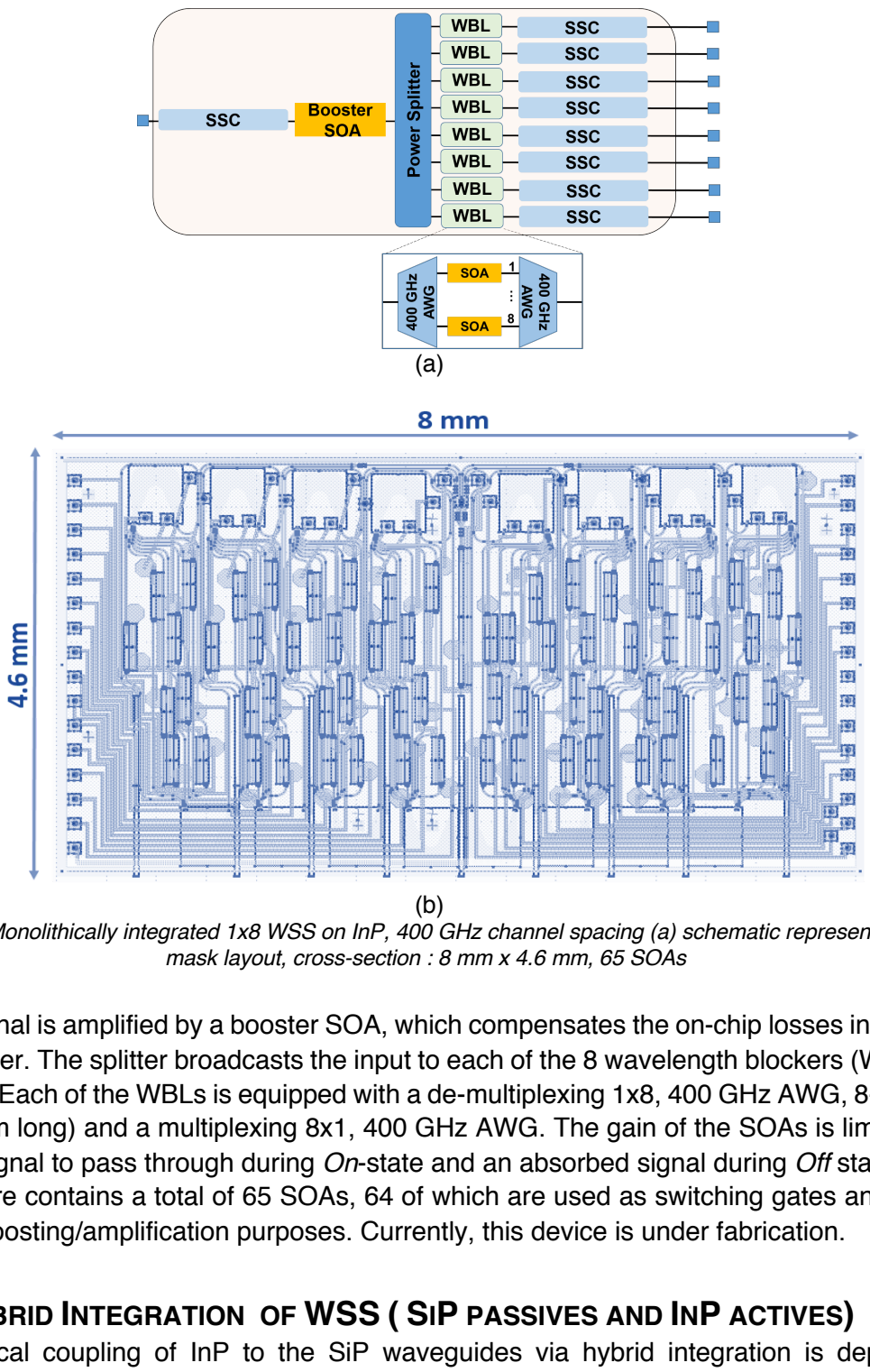


Figure 5. Monolithically integrated 1x8 WSS on InP, 400 GHz channel spacing (a) schematic representation (b) mask layout, cross-section : 8 mm x 4.6 mm, 65 SOAs

The input signal is amplified by a booster SOA, which compensates the on-chip losses including that of a 1x8 splitter. The splitter broadcasts the input to each of the 8 wavelength blockers (WBL), at the output ports. Each of the WBLs is equipped with a de-multiplexing 1x8, 400 GHz AWG, 8-SOA gates (each 500 µm long) and a multiplexing 8x1, 400 GHz AWG. The gain of the SOAs is limited to only enabling a signal to pass through during *On*-state and an absorbed signal during *Off* state. The 1x8 WSS structure contains a total of 65 SOAs, 64 of which are used as switching gates and one SOA is used for boosting/amplification purposes. Currently, this device is under fabrication.

2.2 HYBRID INTEGRATION OF WSS (SIP PASSIVES AND INP ACTIVES)

Efficient optical coupling of InP to the SiP waveguides via hybrid integration is dependent on alignment with precisions in the lower micrometer or even sub-µm range. Active alignment technques proves to be time-consuming and expensive technique. Rather, passive alignment technique conducted by using high precision mechanical placement of the chip can generate optical packaging with a coupling loss less than 2 dB/facet. Flip-chip bonding of InP chip onto SiP provides an efficient electrical interconnection system via solder bumps structure on the chip and a bonding

material on the substrate. Furthermore, unlike wire bonding, it provides high density electrical interconnection there by allowing for reduced die size.

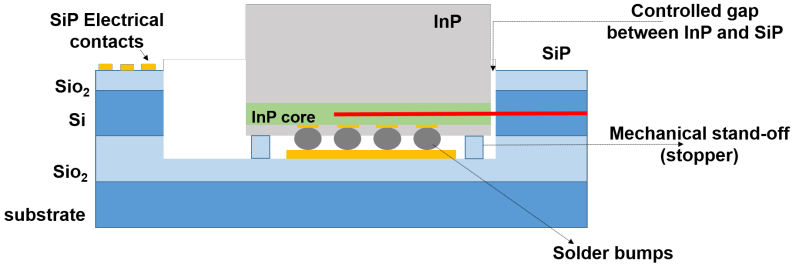


Figure 6 . Cross-section view of the flip-chip bonding assembly of InP chips on SiP cavity

Therefore, for the hybrid integration of the WSS, a flip-chip bonding with a well controlled passive opto-mechanical alignment technique developed by a partner institution VTT will be followed. In order to minimize the coupling loss, the waveguide modes of the two chips must be matched. For this, good control of the lateral and vertical off-set has to be minimized and the gap between the chips has to be well controlled. A vertical alignment/positioning accuracy of less than ± 0.5 μm is required. It is possible to directly bond the InP chip and the SiP together via a thermal compression (TC) technique [6]. In TC bonding, the Au-coated contact pads of the InP and SiP chips are bonded together with the combined effect of elevated temperature (typically >300°C) and bonding pressure. The good control in the thickness of the deposited thin films and the Silicon oxide stoppers then provide excellent vertical alignment [7]. The cross-section view of the flip-chip assembly to be employed is shown in Fig. 6. The InP chip will be flipped down onto SiP cavity, where the solder bumps will be used for electrical bonding.

After flip-chip bonding, the electrical contacts are routed to the top of SiP chip for wirebonding with the external power supply. The mechanical stopper is used to vertically position/align the core of the InP waveguide to that of the waveguide core in SiP. Better alignment tolerance is expected for wider waveguide widths of the SiP chip. Simulations of the coupling efficiency between InP and SiP chips for different length of the gap between the chips (Lgap) is carried out for a 1.8 μm and 3 μm SiP waveguides respectively as shown in Fig. 7(a) and Fig. 7(b). It can be seen that the closer the two chips (for smaller L_{gap}), better coupling efficency is obtained. Due to better mode matching of a 1.8 μm thick SiP waveguide, higher coupling efficiency is achieved. However, higher coupling loss is incurred for a small increase in L_{gap}. Due to broader mode field of the 3 μm thick SiP waveguide, a better tolerance with respect to L_{gap} variation is observed as shown in Fig. 7(b). Therefore, by keeping the gap between the InP and SiP chips L_{gap} to 2 μms and less, an efficient coupling of 3 μm thick SiP waveguide is achieved. Based on these results, the design of the agile WBL makes use of 3 μm thick SiP waveguides.

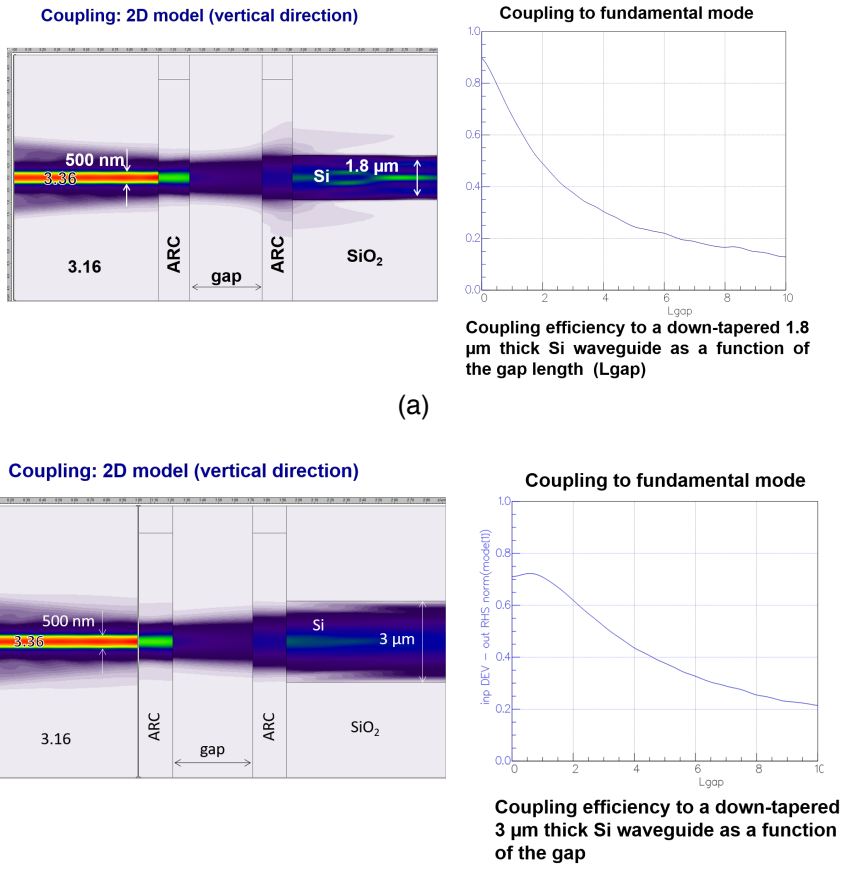


Figure 7. Simulation on fundamental mode coupling of InP waveguide (500 nm thick core) (a) for a 1.8 µm thick SiP waveguide (b) for a 3 µm thick SiP waveguide

Fig. 8(a) and (b) show the cases of coupling InP chip onto SiP from both sides. Under the ideal scenario, an InP chip will be cleaved accurately and the dimension will be the nominal design value *Y*. By controlling the gap between InP and SiP accurately, efficient coupling can be achieved. However, in practice, cleaving tolerance of δY upto $\pm$ 20 μm is introduced, which can make the coupling loss very high or impossible in case of larger or smaller InP chip size. Therefore, to solve this, the same side coupling schematically represented in Fig.8(c) will be adopted. In this case, regardless of the cleaving inaccuracy of the InP chip, efficient coupling can be realized by controlling L_{gap} only from one side and on the opposite side SiP will be etched to accomodate any length

variation that happens on InP chip due to cleaving inaccuracy. The schematic representation of a hybridly integrated WBL structure, with SiP passives and SOA actives is shown in Fig.8(d). The schematic shows the flip-chip bonding result of an InP SOA array chip on SiP chip containing passive deMux/Mux pair. A WDM input signal to the hybridly integrated chip first passes through the deMux circuit. The individual wavelengths are then connected to the SOAs on InP chip whose outputs are coupled to the Mux circuit on SiP chip. For a deMux with *N* channels, an *N* SOA array chip is used. The Mux output is coupled out of the SiP chip. The deMux/Mux circuit can be based on an AWGs or

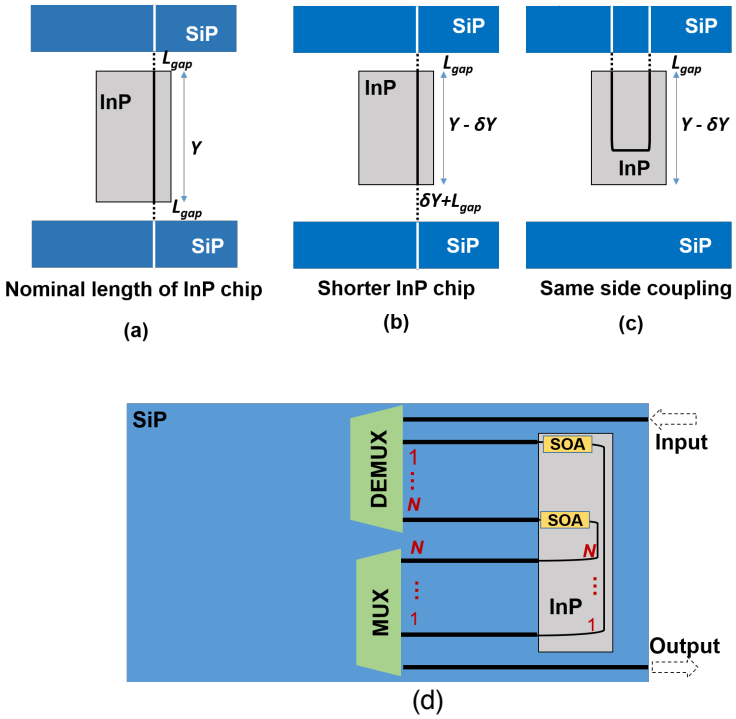


Figure 8. Schematic representation of (a) two side InP chip on SiP cavity, nominal length of InP chip (b) two side InP chip on SiP cavity, shorter length of InP chip (c) InP chip with the all I/Os on the same side (d) hybrid integrated WBL after flip-chip bonding (passive SiP deMux /Mux units and active SOA chips)

Echelle Gratings.

2.2.1 Wavelength blocker (WBL) Design

In order to realize the target implementation of PASSION agile WSS units with 100 GHz spacing and 40 channels, as a first step, 100 GHz WBL structures with 10 channels are designed in SiP chip on top of which InP SOA arrays will be flip-chip bonded. Two variants of the WBL with relative central wavelength shift of 25 GHz are designed. The 25 GHz relative wavelength shift is targeted at spectral spacing of the agile WSS functionality. The specification of these WBLs is listed in Table.1. The schematic of the passive deMux/Mux structure for the integrated WBL and InP SOA array is found in Fig. 9.

Table.1 List of hybrid integrated WBL design structures

Functional Structure	Features	Components
1	10 channel WBL , 100 GHz spacing Center wavelength : 1546.52 nm	- Two 1 x 10 AWG, 100 GHz spacing - 10 SOA arrays on InP
2	10 channnel WBL , 100 GHz spacing Center wavelength :1546.72 nm	- Two 1 x 10 AWG, 100 GHz spacing - 10 SOA arrays on InP

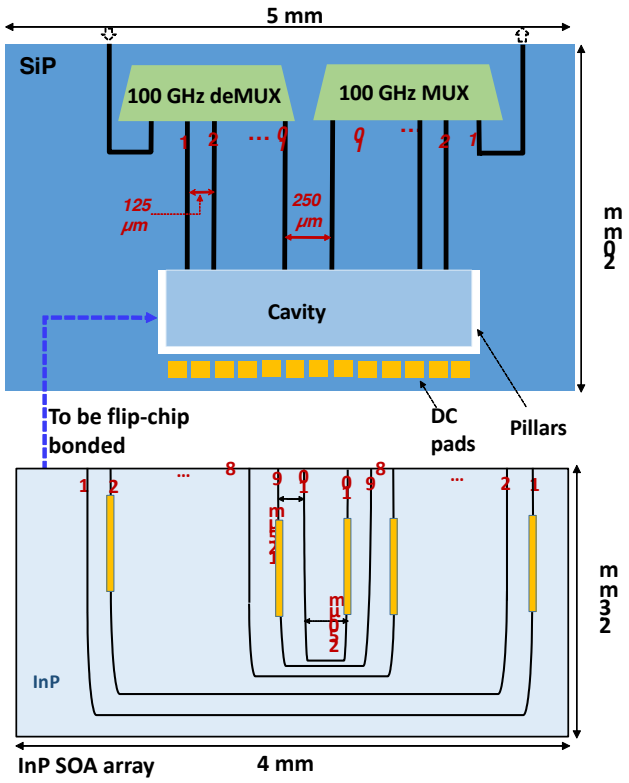


Figure 9. Schematic of two hybridly integrated WBLs, 100 GHz channel spacing (SiP AWG 1x10 deMux and 10x1 AWG Mux , InP 10 SOA array chip)

Two of the 100 GHz deMux/Mux AWG device (each 3 x 2.8 mm^2) as indicated in Fig.9 are layed on the north edge of the chip. In south edge of the SiP chip a cavity for holding the InP chip is designed. The output of the deMux and inputs of Mux are connected to waveguide arrays which in turn will be coupled to InP chip upon flip-chipping. An input waveguide to the WBL is de-multiplexed into 10 output waveguides of a 100 GHz deMux. Ten straight waveguides are routed to the SOA array chip which serve as ten SOA gates. The outputs of the SOA chips are then connected to the multiplexing AWG by 10 straight waveguides. The 4 x 2.3 mm^2 SiP cavity is designed to be used for flip-chip bonding of InP SOA array chip of same size. Therefore, pillars of width of 100 μm are built around the 3 edges of the cavity. The SOA array are connected with U-shaped waveguide to enable one side coupling of light. The input/output waveguide pitch on the two chips is designed to match the value of 125 μm. The waveguides arrays of the de-Multiplexer and multiplexer are separated by 250 μm. The optical input/output interfaces of the WBL are found in the north edge of the chip. Thus, the output waveguide of 100 GHz Mux AWG is routed to the north edge of the chip as output of the WBL. At the bottom of SiP cavity, electrical DC contact pads are placed with a pitch of 250 μm.

2.2.2 Array waveguide gratings (AWG) and Echelle grating (EG) Designs

Table. 2 lists the design specification of the AWG incorporated within the WBLs. Two of these AWGs will be used in a single WBL, resulting in a total of 5 dB of the insertion loss in SiP passive. These losses will be compensated by the SOA array chip.

Table. 2 Design specification of 10 channel AWG used as de-Multiplexer and Multiplexer in WBL

Design specification of AWG	Value
Number of channels	10
Channel spacing (GHz)	100
3dB bandwidth (GHz)	50
Extinction ratio (dB)	>25
Insertion loss (dB)	< 2.5

The above presented AWG design has a Gaussian passband. One of the limitation in the correct operation of the WBL based on these AWGs is the central wavelength mismatch between the deMux/Mux AWGs. This is caused by small deviation in the refractive index, inherent to current fabrication technologies. One solution is to design flat passband AWG so that the behaviour of the AWG remains unchanged for small deviations while, at the same time, inter-channel cross-talk is being minimized.

An alternative solution is to use a single device as deMux/Mux device. For this purpose, single Echelle grating (EG) to perform the de-multiplexing/multiplexing operations prior and posterior to the InP section of the WBL is designed. The geometry of EG guarantees that fabrication errors will be equal for the de-multiplexing and multiplexing process at the expense of a larger area, a very important trade off on integrated photonics. Fig. 10(a) shows a schematic of the design of a 3x25 EG with channel spacing of 100 GHz. This device will serve as both de-Multiplexing and multiplexing device. The first input will serve as the input of the deMux, and outputs 1 - 10 will serve as outputs of the de-multiplexer. Outputs from 16 -25 will serve as inputs to the multiplexer. Therefore, outputs 1 - 10 of EG will be connected to 10 SOA array of the InP chip, whose outputs will inturn be connected outputs 16-25 of the EG. Thus, one EG connected to 10 SOA array chip will emulate the functionality of a WBL. Fig. 10(b) shows the mask layout of the EG, which occupies an area of 8x8 mm^2.

Fig.10 (c) and (d) shows the initial simulation results of channels 1-11 and 15-25, which are spectrally aligned and can serve as deMux/Mux pair of the WBL. The remaining waveguides are then used for calibration. Although, EG provides a fabrication tolerant Mux-DeMux with very low insertion loss, it is necessary to route correctly the inputs and outputs since the positions on the outputs are not mirror

symmetric. Thus a set (9) of waveguide crossings would be required, increasing the insertion loss to a similar level of an AWG.

2.2.3 InP SOA array

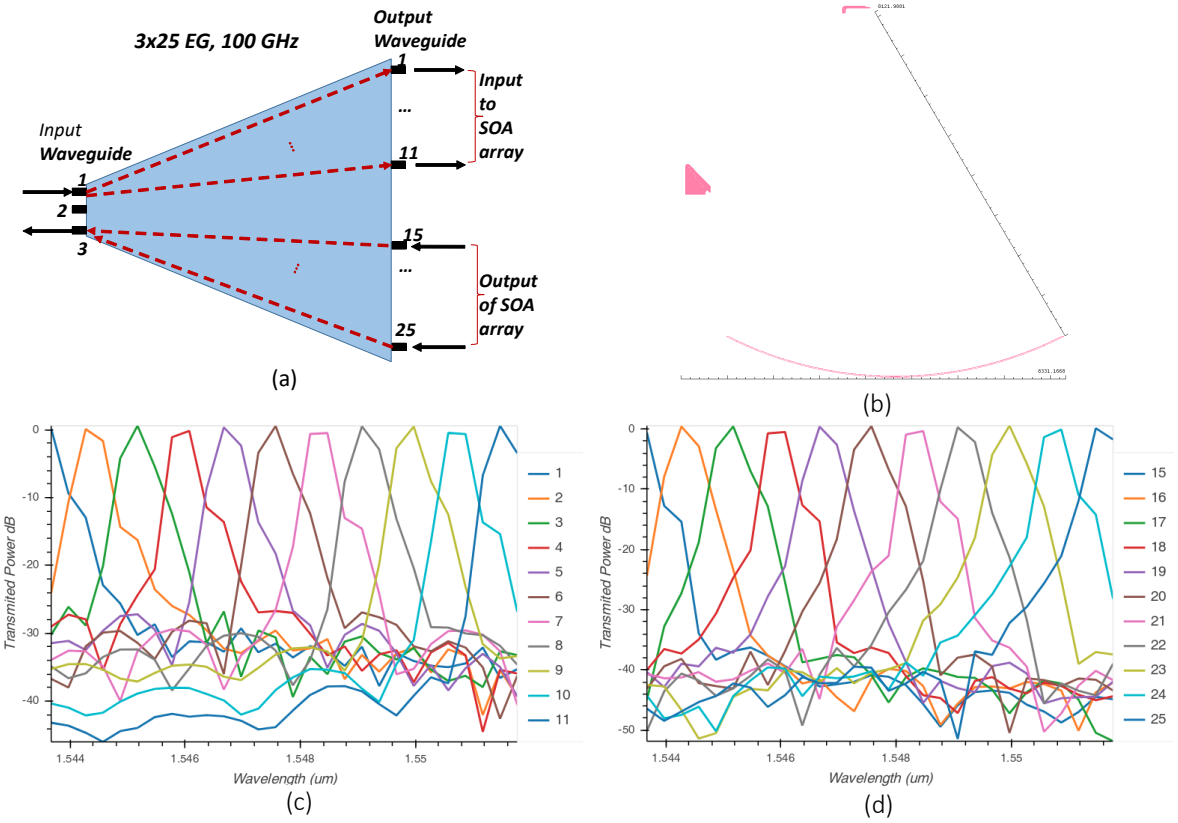


Figure 10. (a) Schematic of 3x25, 100GHz Echelle grating with 3 input waveguides and 25 output waveguides (b) mask layout of EG design (c) Transmission response from output waveguide 1 -11 (d) Transmission response from output waveguide 15 -25

Arrays of 900 μm long SOAs are designed to be used as both booster and gate SOAs. The gain of the gate SOAs is used to compensate the on-chip losses of SiP passives and the gain of the booster SOAs compensate small values of coupling losses. As a result the SOAs, will be biased with low bias current, thereby reducing the power consumption of the WSS. Furthermore, when the SOAs are pumped with low bias current, the heat output of the SOAs is also lowered. This in turn leads to low power consumption of Thermo-electric cooler (TEC), which is equivalent to low power consumption of the WSS. The design specification of the InP SOA array are listed in Table. 3.

Table 3. Specification of InP SOA array

Design specification of SOA	Value
Length (μm)	900
gain needed for operation(dB)	6
Pump current (mA)	40
Extinction ratio (dB)	>40

3 CHIP DESIGN FOR HYBRID INTEGRATION

Flip-chips are an advanced form of surface mount technology in which bare semiconductor chips are turned upside down and bonded directly to a printed circuit board or chip carrier substrate. Interconnection between the chip I/O and substrate is achieved using a bump structure on the chip and a bonding material-typically on the substrate. The bumps can be solder or a conductive adhesive. Solder bump flip-chip interconnections were developed to eliminate the expense, unreliability and low productivity of manual wire bonding. In contrast to wire bonding, the flip-chip allows all I/Os to be connected simultaneously. This allows for high I/O counts at large pitches and reduced die size because solder bumps can be put over the entire active device area.

Therefore, in the context of this deliverable, InP chip design at Tu/e and SiP cavity design at VTT and have been carried out for the hybrid integration of agile WSS via flip-chipping.

3.1 INP MASK DESIGN

SOA arrays containing 12 SOAs is designed in a 4x2.3 mm^2 InP chip. The schematic representation and the mask layout of the SOA array chip is shown in Fig.11 (a) and Fig. 11(b). The optical input /output waveguides are all put in one side, in the left side of the chip. The pitch between adjacent

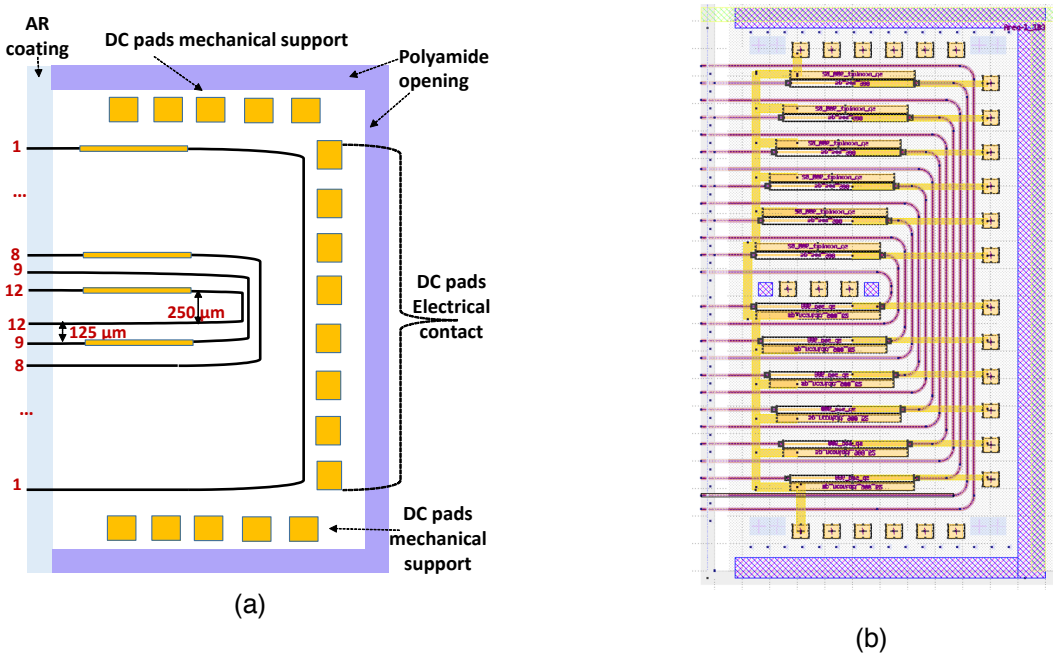


Figure 11. 12 SOA array InP chip (a) schematic representation (b) mask layout, cross-section : 4 mm x 2.3 mm

waveguides is 125 μm. A minimum separation of 250 μm distance is kept between two adjacent SOAs. The electrical contact pads of the SOAs are put in the right edge of the chip. At the bottom, middle and top portions of the chip, DC contact pads are put for mechanical support purposes to be used while flip-chip bonding. For successful coupling of light from SiP chip to flip-chip bonded InP chips, it is very important to maintain the vertical alignment with a maximum tolerance of ±0.5 μm. The topmost layer of the InP chip (polyamide layer) creates irregularities on the surfaces of the InP chip. Therefore, it is important smooth out irregularities on the surface of the InP chip where it makes physical contact with the pillars on SiP cavity. As can be seen in Fig. 11 (a) and Fig.11 (b) a strip of

polyamide opening is put in all sides of the chip excluding the side containing the optical input/output facets. The dimensions of the polyamide openings are listed in Table. 4. In addition, to facilitate the optical alignment in the lateral directions, cross-shaped alignment markers are etched into the four corners of the InP chip. Triangular shaped markers in the top and bottom of the InP chip. The InP chips are equipped with anti-reflection coating to minimize reflection of light at the input/output waveguide facets.

The layer stack of the InP SOA chip as depicted in Fig.12 is taken into account for SiP cavity design to be used for flip-chip bonding. The InP waveguide core of 0.5 μm thick is situated 1.75 μm below the indicated point (*Ref level). The electrical DC pad are situated 6.55 μm above the centre of the waveguide core. The overall thickness of the InP chip is about 200 μm.

Table. 4 Dimensions of Polyamide openings on InP SOA array chip

Item	Width (μm)	length (μm)
Top side polaymide opening	100	2150
Bottom polyamide opening	100	2150
Right side polyamide opening	150	4000

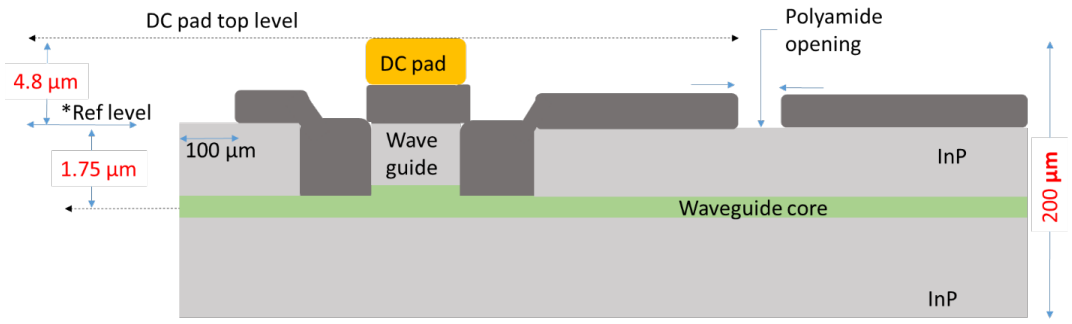


Figure 12. InP layer stack

3.2 SiP CAVITY DESIGN

The SiP cavity is designed complimentary to the InP chip, and a schematic of the intended flip-chip bonding process is shown in Fig.13. The depth of the cavity is adjusted so that the optical axis of the InP waveguide core aligns with that of the SiP waveguides after flip-chip bonding. The cavity has vertical stoppers on three sides so that the waveguide cores are self-aligned during assembly.

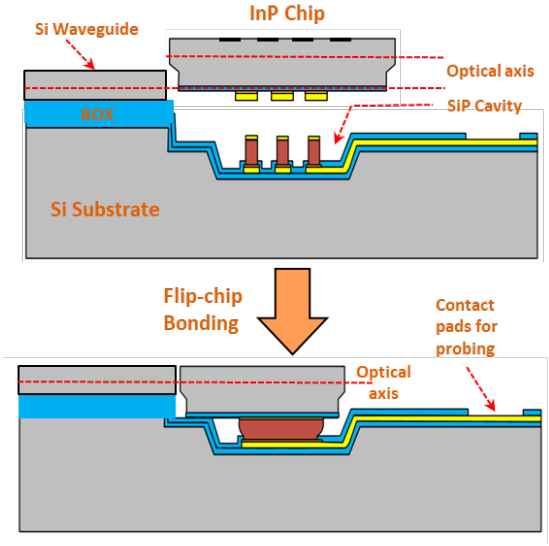
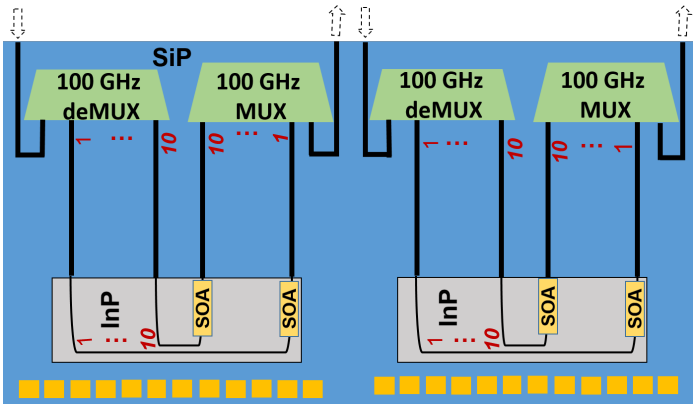


Figure 13. Schematic of the flip-chip bonding process



(b)

Figure 14. (a) mask layout of the SiP chip for two WBL (2 deMux/Mux AWG pairs, with 10 channels) (b) Schematic of the hybrid integrated WBL (to be realized after flip-chip bonding of the SiP with InP SOA arrays)

Alignment in the lateral direction is achieved with U-bend waveguide that start out as straight waveguide on the SiP chip, continue into the InP chip where they execute the U-bend, and exit back into the SiP chip. Metal pads, complimentary to the ones on the InP chip, are defined at the bottom of the SiP cavity. They will be utilized during the flip-chip bonding, and also for making electrical connections to the InP chip. Metal lines with a pitch of 250 μm run out of these metal pads, and are routed to the south edge of the SiP chip for probing purposes.

The finalized layout of the SiP mask design is shown in Fig.14 (a). Two pairs of deMux/Mux corresponding to the two WBL are situated in the north edge of the chip. Eight waveguides corresponding to optical input/output of the two WBLs and test waveguides are put with a pitch of 1000 μm for easier accessiblity while fiber pigtailing. The array waveguides connected with deMux

and Mux AWG are guided to the SiP cavity where the InP SOA chip will be placed. By taking into account the impact of heat dissipation from the SOA array chip, the cavity is placed as far away from AWG deMux/Mux as possible.

Fig. 14(b) shows the schematic of the hybridly integrated agile WSS chip expected to be realized after flip-chip bonding. The heat output the SOA arrays will be extracted via TEC placed at the bottom of the SiP chip. Upon flip-chipping, the heat flow will be directed away from the InP SOA array through SiP cavity down to the heat sink.

4 CHARACTERIZATION RESULTS OF WBL ELEMENTS

4.1 SYSTEM CONCEPT

The proof of concept experimental demonstration of a 1x2 WSS makes use of a 1x2 splitter and two wavelength blocker (WBL) as presented in Fig.15. The WBL will be constructed from a de-multiplexer based on VTT's SiP AWG/EG. The output waveguides of the de-Multiplexer outputs are connected to a discrete SOA array, which are used as a switching gates in a WBL operation. The outputs of the SOA arrays are later combined by a commercial multiplexer.

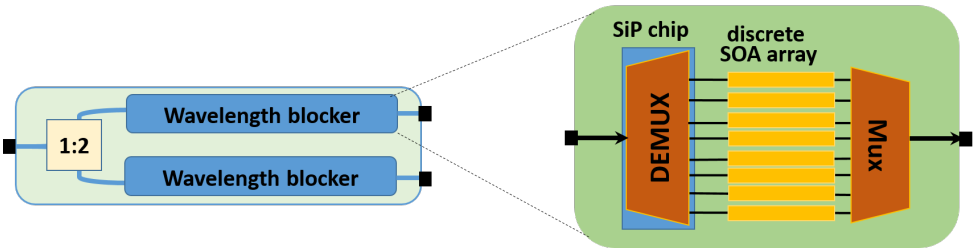


Figure 15. Schematic representation of a 1x2 WSS, with SOA based wavelength

In the next section, the characterization results of on-chip AWG/EG and discrete SOA arrays are presented.

4.1 SIP PASSIVES (EG AND AWGS)

The SiP passive designs of a 100 GHz, 40 channel AWGs and EGs designed and fabricated at VTT. The characterization result measured on optical fiber alignment stage are given next subsection.

4.1.1 100 GHz EG with 40 channels

A1x8 100 GHz, EG cascaded by 1x5 800 GHz EG structure is designed to generate 40 channels with 100 GHz spacing. One of the advantages of EG is that their performance and the area they occupy is not affected by the number of outputs. Thus, an EG that demonstrates a good performance for multiplexing or de-multiplexing at 100GHz with sufficiently good polarization independency, will maintain these properties for a larger number of outputs. Fig. 16 shows the transmission response of 1x8 100 GHz EG.

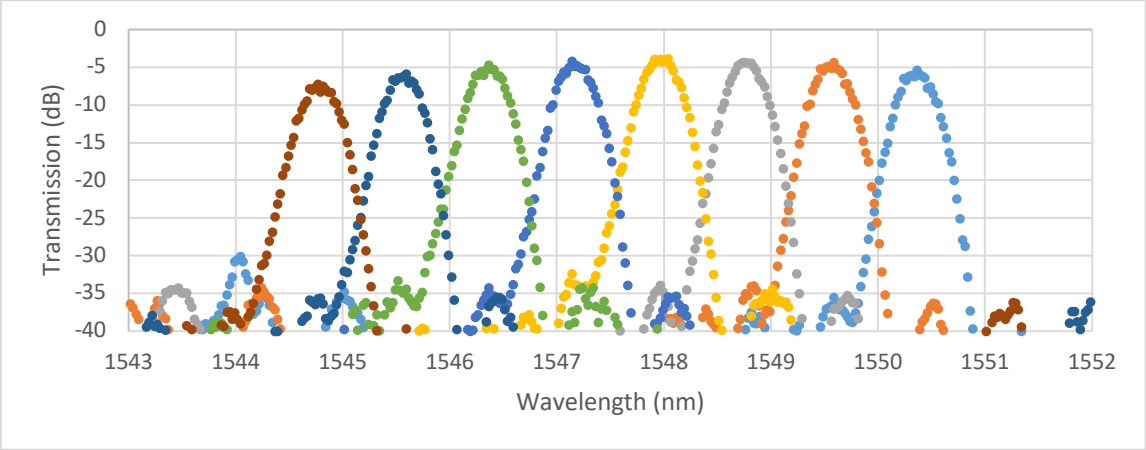
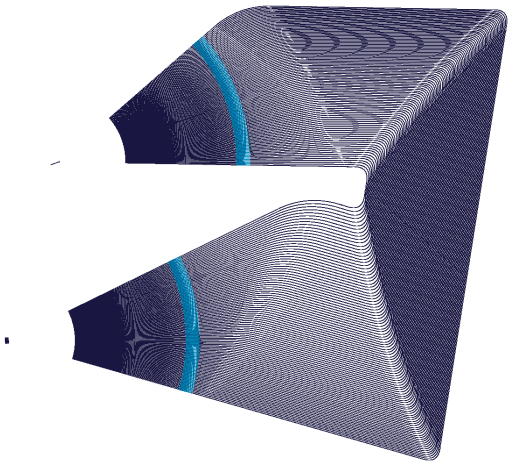


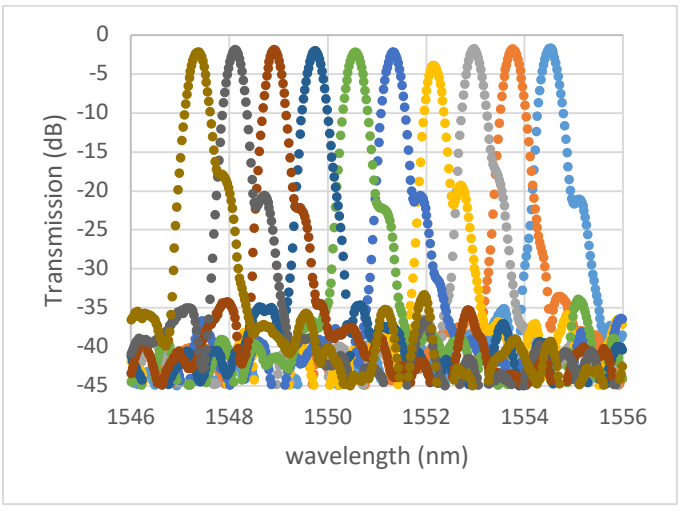
Figure 16. Measurement results on the 1x8 EG with 100 GHz spacing

4.1.2 100 GHz AWG with 40 channels

Within the PASSION project, there already exists successfully designed and tested 1x10 and 1x40 AWG component with a 100 GHz channel spacing. The 1x10, 100 GHz AWG device shown in the Fig.17 (a) has a footprint of 3 mm x 2.8 mm, and the measured characteristics of this device is also shown below Fig.17 (b). It has similar design specification as the AWG design presented in section 2.2.2. The measurement results show that insertion loss of the channel is on average less than 3 dB. Fig. 18 shows the transmission response of the AWG for all 40 channels.



(a)



(b)

Figure 17. (a) mask layout of 1x10, 100 GHz AWG (b) Measurement results on the 1x10 AWG with channel spacing of 100 GHz

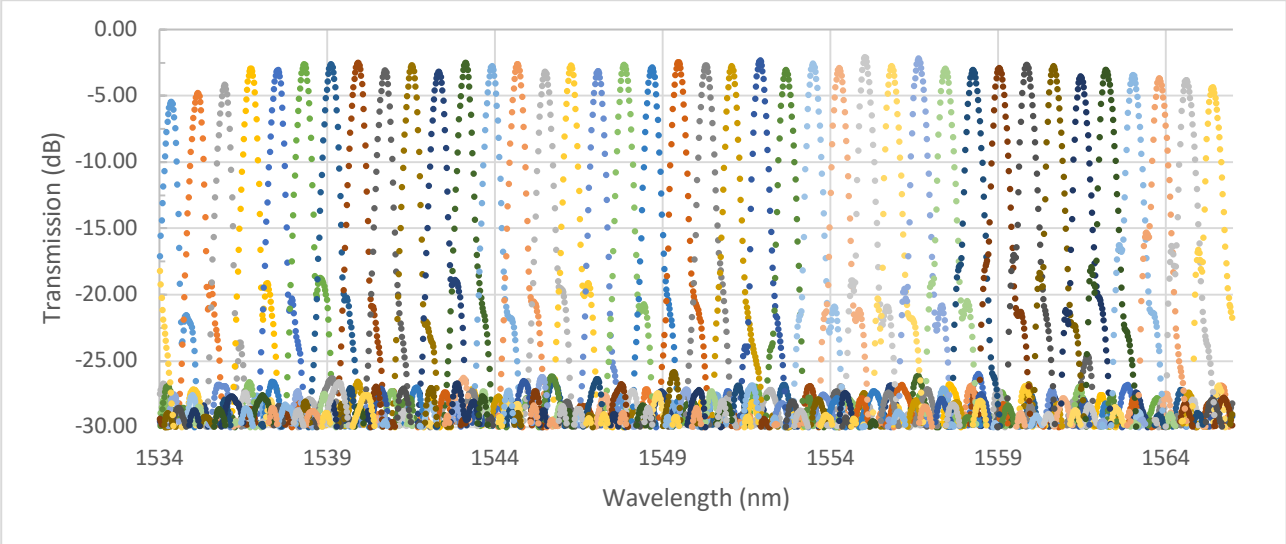


Figure 18. Measurement results on the 1x40 AWG with channel spacing of 100 GHz

Looking at the results presented in Fig.16, 17 and 18, it can be seen that good performance is recorded for all channels. The cross-talk level is below -25 dB in all cases. The insertion loss of the presented SiP AWG and EG is on average in the order of 3 dB. The deMux/Mux circuit will have a maximum of 6 dB of insertion loss. This means the gate SOAs will need to provide a maximum gain of 6 dB proving the capacity to implement low-power consumption WSS using SiP passives.

4.2 DISCRETE SOA ARRAYS

Discrete SOA arrays will be used as switch gates in the proof-of-concept implementation of hybrid WBL. The performance of the SOAs is characterized with regard to gain and output OSNR for

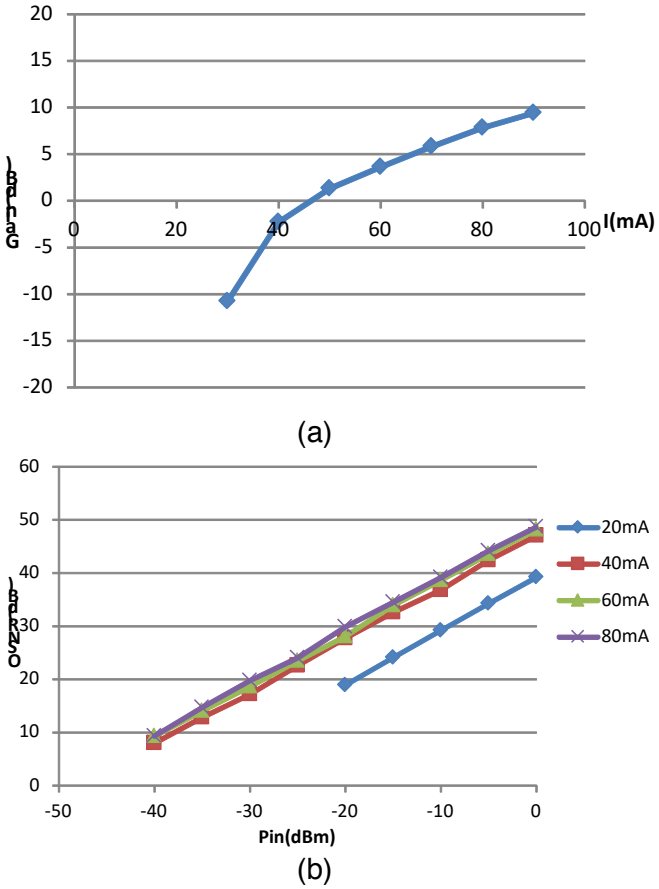


Figure 19. Discrete SOA measurement results (a) gain (dB) vs bias current (mA) of the SOA (b) OSNR (dB) versus input power for different values of bias curent (mA)

different values of bias current (mA) and input power, as demonstrated in Fig. 19. As can be seen in the Fig. 19 (a), for low values of the bias current, the SOA has negative gain, i.e. it (attenuates) absorbs the input light. For bias current value above 45 mA (threshold current), positive gain is achieved. Gain up to 10 dB is achieved when the bias current is increased to 90 mA.

Fig. 19 (b) shows OSNR output of the SOA for different values input power and bias current. It is obvious from this figure, for the same value of output OSNR, higher input power into the SOA corresponds to lower bias current, therefore achieving/enabling low power consumption. Therefore, by reducing fiber-to-chip coupling losses via hybrid integration, low-power consumption of the WSS is achieved.

These initial preliminary tests on SiP passives and discrete SOAs prove the capability to implement low-power consumption agile WSS.

5 CONCLUSIONS

In this deliverable, the implementation of low-power consumption agile WSS with both monolithic integration in InP and hybrid integration InP and SiP is reported. The agility of the WSS is implemented by following dense spectral grid of 25 GHz combined with dynamicity both in wavelength and channel bandwidth.

The realization of low power consumption WSS is sought by aggressive optical loss reduction within the WSS circuit. In case of monolithic integration this is achieved through the use of spot-size converter InP waveguides for coupling loss less than 2dB/facet. The design of functional 1x8 InP WSS is already carried out, and the circuit is under fabrication. In case of hybrid integration, flip-chip technology from VTT will be used to achieve coupling loss of less than 2 dB/facet. Accordingly, SiP passives namely Arrayed waveguide gratings (AWGs) are designed to serve as deMux/Mux circuit of hybrid WBL. Similarly, arrays of Semi-conductor optical amplifier (SOAs) to be used as gate switches of hybrid WBL are designed and are currently under fabrication. In preparation for the flip-chip bonding activity, cavity design on SiP chip and mask-co design of InP chip has been done.

Furthermore, design of new type of Echelle grating (EG) that is intended to avoid the relative wavelength mismatch between the deMux and Mux of the WBL is given. In this new presented design, a single EG will be used to serve as de-multiplexer and multiplexer.

In addition, the characterization result of the SiP EG and AWGs is presented. The performance of these passives is promising and verify that it is possible to achieve low power consumption WSS via low-loss integration of passives with SOA arrays.

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7 ACRONYMS

AWG	Arrayed waveguide grating
EG	Echelle grating
InP	Indium phosphide
OSNR	Optical signal-to-noise ratio
PIC	Photonic integrated chips
SDN	Software defined network
SiP	Silicon Photonics
SOA	Semi-conductor optical amplifier
SSC	Spot-size converters
TC	Thermal compression
WBL	Wavelength blocker
WDM	Wavelength division multiplexing
WSS	Wavelength selective switch